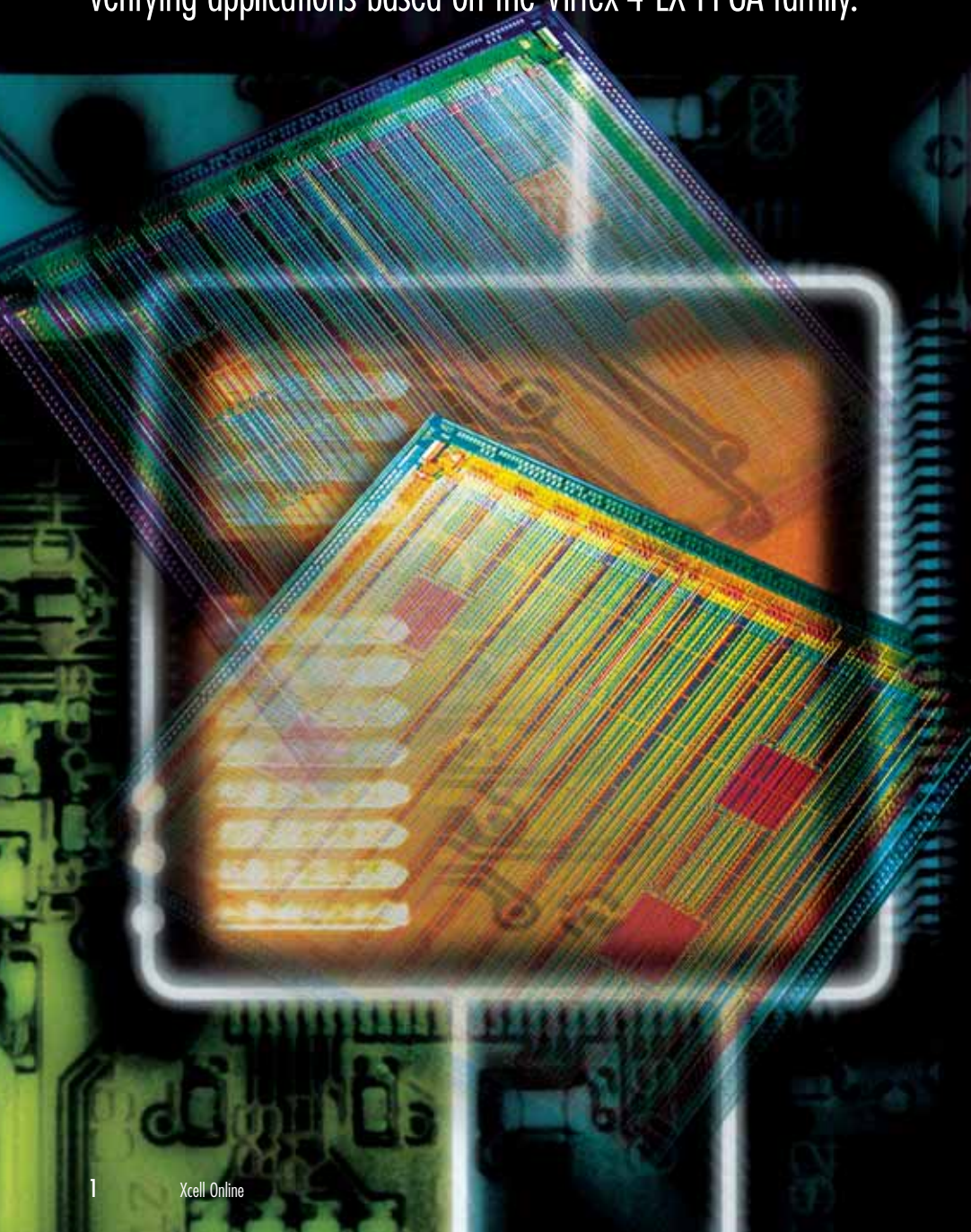
Virtex-4 Source-Synchronous Interfaces Tool Kit

The Virtex-4 ML450 Source-Synchronous Interfaces Tool Kit provides a complete development platform for designing and verifying applications based on the Virtex-4 LX FPGA family.



by David Naylor
Sr. Product Applications Engineer
Xilinx, Inc.
david.naylor@xilinx.com

Many of today's telecom and networking systems use high-bandwidth interfaces based on low voltage differential signaling (LVDS) or other differential I/O standards. Differential I/O standards simplify system design by improving system performance and signal integrity.

Protocols based on I/Os such as SPI-4.2, SFI, RapidIO, and HyperTransport are central to leading-edge system design. To take advantage of these technologies, you have to work through multiple challenges to ensure device interoperability and standards compliance.

Xilinx® provides Virtex™-4 development boards as well as standards-compliant intellectual property (IP) cores and free reference designs for major system interface protocols. This allows you to focus on user application design and not worry about interoperability and standards compliance.

With the Virtex-4 source-synchronous interfaces tool kit, designing networking, telecom, servers, and computing systems has never been faster or easier.

The Virtex-4 ML450 source-synchronous interfaces tool kit includes the following:

- Virtex-4 ML450 development board (XC4VLX25FF668 FPGA)
- 5V/6.5 AC/DC power supply
- Country-specific power supply line cord
- RS232 serial cable, DB9-F to DB9-F
- Four clock module daughter boards
- Two sets of "blue ribbon" loopback cables for LVDS testing
- Documentation and reference design CD-ROM

The Virtex-4 ML450 Development Board

The main component in the Virtex-4™ ML450 source-synchronous interfaces tool kit is the ML450 development board (Figure 1). Featuring a Virtex-4 XC4VLX25FF668 FPGA coupled to high-speed connectors, this board supports the development of high-speed interface designs using several popular protocols.

The ML450 demonstration board is a simple board providing several connector interfaces to the FPGA. The board comprises basic support circuitry, including power regulators, a serial RS232 connector, a small graphics LCD, a few user push buttons and LEDs, and a DDR-1 SDRAM. These simple peripherals allow a PC to communicate with the FPGA and also provide basic input and output indicators. Configuration is enabled via a JTAG connector, or you can use a System ACE™ CompactFlash card for bitstream storage and loading.

We designed the board to demonstrate the high-speed I/O capability of the Virtex-4 FPGA. Eighty differential channels are pinned out to four Samtec connectors. Forty pairs each are routed to two connectors on either side of the FPGA, allowing you to designate "transmit" and "receive" interfaces. Two "mini coax" flat cables are provided with the kit, enabling loopback of high-speed data between transmit and receive connectors.

In addition to these differential signals, another 32 pairs are routed to a HyperTransport Consortium DUT (device under test)-compliant connector, allowing for the development of an interface to other HyperTransport-based boards.

The ML450 evaluation platform supports a wide range of communications standards, including SFI-4. Figure 2 shows the user interface of an SFI-4 demo running on an ML450 board. The user interface includes a bit error rate tester (BERT) that measures the integrity of the data received from 16 LVDS transmitters. You can select from several pseudo-random bit sequences to simulate data, and error counters on the user interface maintain a running count of all bit errors that occur during transmission. The BERT also keeps track of which channels are receiving errors to provide further troubleshooting visibility in a multi-channel design.

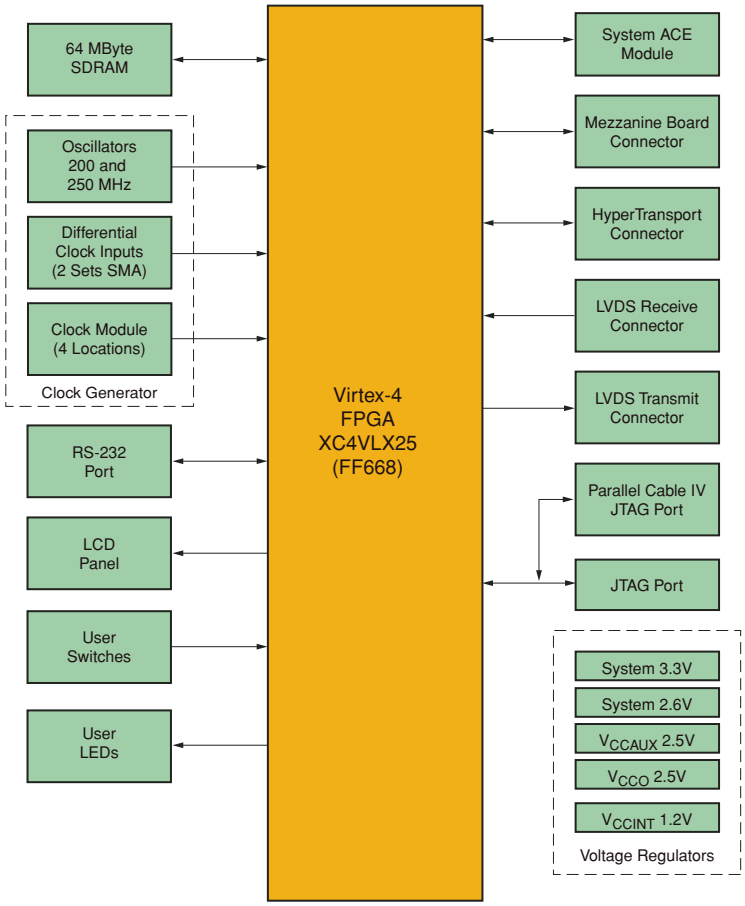


Figure 1 – Virtex-4 ML450 networking interfaces development board

In terms of performance, the ML450 platform supports a 16-channel single data rate design (SDR) running up to 700 MHz (Figure 3) and a 16-channel double data rate (DDR) design running up to 500 MHz (Figure 4). The transmission medium of the 16 channels consists of two Samtec connectors, a 12-inch ribbon cable, and 10 inches of FR4.

The ML450 also provides the ability to command the supply rails of the FPGA to assume +/- 5% of their nominal values. This feature provides a convenient way for you to stress your design and identify marginal behavior. The voltages are controlled through the user interface by simply moving a slider button to the left or right. In Figure 2, VccAux is raised to +5%, while the other supplies remain nominal.

A small daughtercard that plugs onto the board provides the high-speed clock used by the SFI-4 design. This daughtercard generates a programmable LVDS clock between 200 MHz and 700 MHz, eliminating the need for a cumbersome bench-top pulse generator.

Board Features

The ML450 development board includes the following:

- XC4VLX25FF668 FPGA
- Eight clock sources:
  - 200 MHz and 250 MHz on-board oscillators
  - Two sets of SMA differential clock input connectors
  - Four Samtec clock module connectors
- One 64 x 128 pixel LCD
- One DB9-M RS232 port
- A System ACE CompactFlash configuration controller that allows storing and downloading of as many as eight FPGA configuration image files

- Four LVDS Samtec connectors (a total of 40 input channels and 40 output channels)
- One HyperTransport connector (HyperTransport Consortium DUT connector-compliant)
- On-board power regulators with ± 5% output margin test capabilities

Clock Generation

The clock generation section of the ML450 development board provides all necessary clocks for the Virtex-4 FPGA. Eight clock sources are provided as follows:

- Epson EG2121CA 2.5V 250 MHz differential low-voltage positive emitter-coupled logic (LVPECL) oscillator
- Epson EG2121CA 2.5V 200 MHz differential LVPECL oscillator
- Two differential SMA clock inputs
- Four Samtec user clock sockets

The differential SMA clock inputs are connected to the global clock inputs of the FPGA, accessing the upper and lower halves. An on-board 200 MHz oscillator calibrates the I/O delay, and an on-board 250 MHz oscillator is provided for use with the HyperTransport IP.

The four clock modules included in the kit are:

- Type A: direct balanced differential SMA input
- Type B: Epson EG2121CA 2.5V 400 MHz differential LVPECL
- Type C: ICS programmable, 200 MHz to 700 MHz
- Type D: unbalanced, single-ended transformer coupled into LVDS

Note that all clock module daughter board outputs are converted to LVDS on the daughter boards.

SDRAM Memory

The ML450 development board provides 64 MB of DDR-1 SDRAM memory (Micron Semiconductor MT46V32M16N-5B).

Figure 2 – BERT user interface

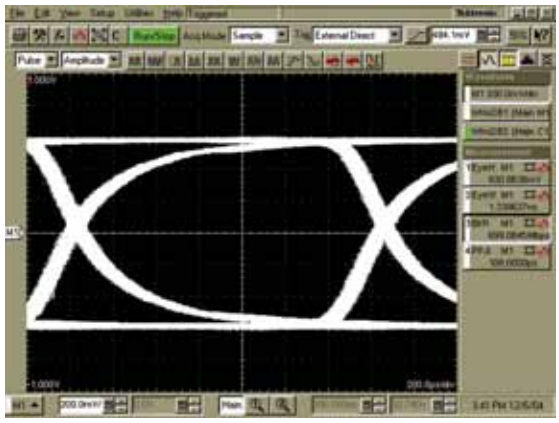


Figure 3 – 700 MHz SDR LVDS eye diagram

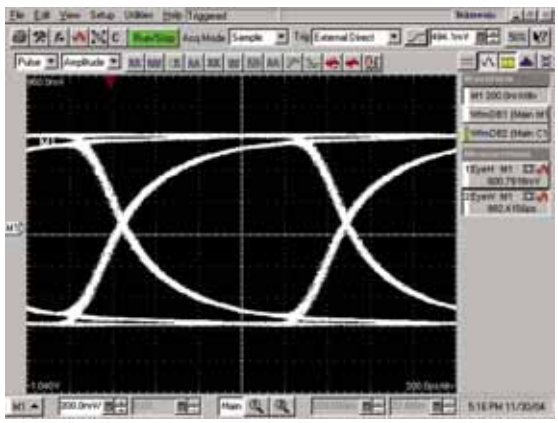


Figure 4 – 500 MHz DDR LVDS eye diagram

Liquid Crystal Display

The ML450 development board provides an 8-bit interface to a 64 x 128 LCD panel (DisplayTech Q64128E-FC-BC-3LP, 64 x 128).

RS232 Port

The ML450 development board provides a DB9-M connection for a simple RS232 port. The board uses the Maxim MAX3316 device to drive the RD, TD, RTS, and CTS signals. You must provide a UART core internal to the FPGA to enable serial communication.

System ACE Interface

In addition to a JTAG configuration connector, the ML450 development board provides a System ACE interface to configure the Virtex-4 FPGA. The interface also gives software designers the ability to run code (for soft-processor IP within the FPGA) from removable CompactFlash cards.

LVDS Connectors

The ML450 development board provides 40 channels of transmit signals and 40 channels of receive LVDS signals. These signals are distributed across two Samtec QSE-DP connectors for transmitting and another two connectors for receiving.

HyperTransport Connector

The ML450 development board provides 16 channels of transmit and receive data, along with miscellaneous control signals on the Samtec QSE HyperTransport connector.

Conclusion

With the Virtex-4 source-synchronous interfaces tool kit, designing networking, telecom, servers, and computing systems has never been faster or easier.

For more information on the demonstration board and the kit, visit *www.xilinx.com/ml450/*.