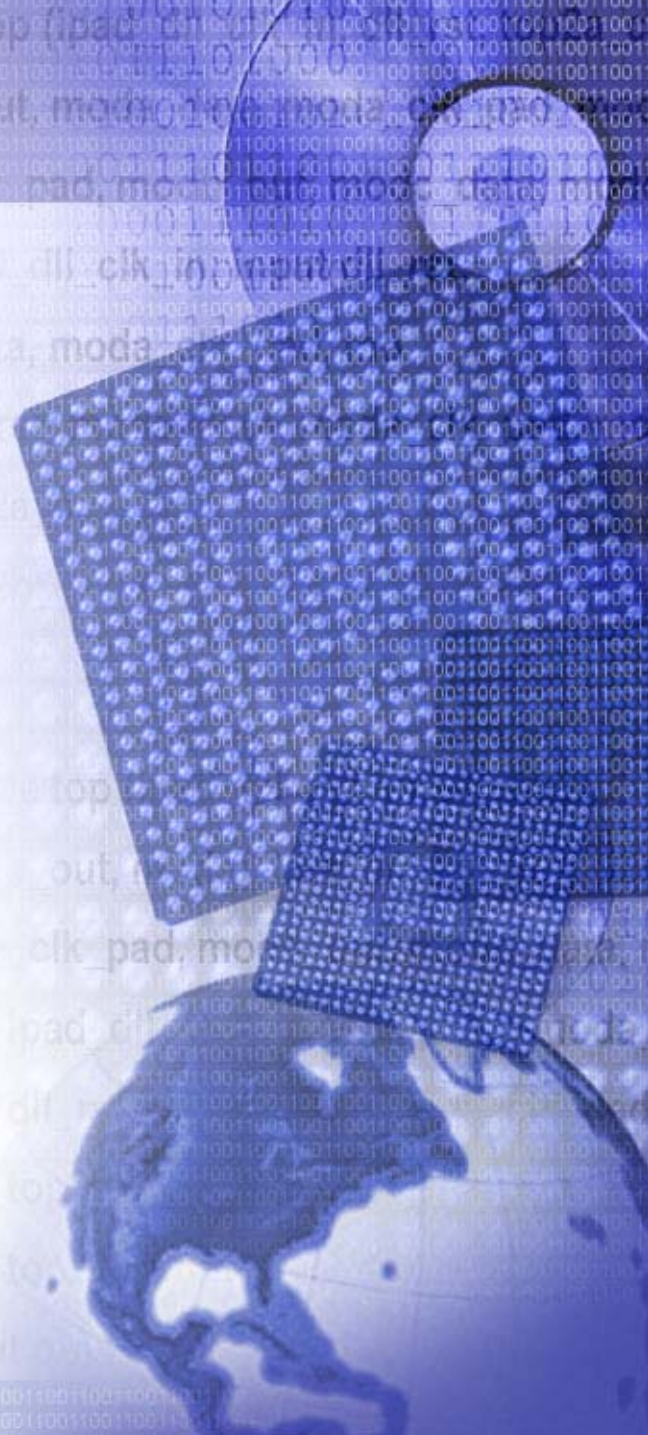
Virtex™-4 Source Synchronous Interface Advantage

High-Performance
Source-Synchronous Interfaces
Made Easy



Key Messages

- Source-synchronous IO (SSIO) techniques have become the norm for building high-speed interfaces
- SSIO design poses new challenges
- Xilinx offers a complete solution for successful SSIO implementation
  - ChipSync™ technology built into Virtex-4 FPGAs
  - Reference designs and IP

Source-Synchronous Interfaces

Key Characteristics

- Point to point connection instead of buses
- Higher chip-to-chip speed
  - SDR: 700 MHz clock
  - DDR: 500 MHz clock
    - 1Gbps data rate
- Higher reliability
  - Minimizes problems of skew and jitter

Applications

- Networking/Telecom
  - SPI-4.2 / SFI-4 / XSBI
  - RapidIO™
  - NPSI (CSIX)
  - Utopia IV
- Memory
  - DDR SDRAM
  - DDR 2 SDRAM
  - QDR II SRAM
  - RLDRAM II
  - FCRAM II

Source-Synchronous I/F Design Challenges

1. Data capture at high speeds
2. Managing clock speeds up to 700 MHz
3. PCB layout challenge
   - I/O placement flexibility
   - Channel to channel skew
4. Implementing multiple interfaces

Virtex-4 Solves SSIO Challenges

- Ensuring reliable data capture at high speeds
  - ChipSync built into every I/O: Clock-to-data centering at “run time”
- Managing clock speeds up to 700 MHz
  - Multiple differential clock distribution networks
  - Clock forwarding with minimal skew and duty cycle distortion
- Simplifying PCB layout
  - IDELAY and BITSLIP in every I/O as part of ChipSync
  - Data agnostic bus alignment and intrusive bit alignment
- Implementing multiple interfaces
  - Abundant clock resources
  - Flexible I/O and banking rules

Source Synchronous Interfaces Made Easy

How to Get Started

- Access latest Virtex-4 source synchronous design solutions on www.xilinx.com/connectivity
  - **IP Cores: SPI-4.2, RapidIO**
  - **Application Notes: SFI-4, XSBI**
  - **ML450 - Source Synchronous Interfaces Toolkit**
    - **Board level solution including: reference designs, schematic & gerber files**
- Contact your local FAE for an on-site demo

Accelerate Your Design Cycle