Department of Electrical and Computer Engineering

COEN 6501 Dec. 10, 2010

Answer all Questions. All Questions carry equal marks

Exam Duration 3 hour

No books or papers are allowed. Lecturer: Asim J. Al-Khalili

Question 1

a) Discuss the merits and disadvantages of programming technologies in FPGAs in terms of speed and area..

b) Implement function F1 using **minimum number of 2:1 MUX**s only. All inputs should be of **non-inverting** type.

$$F1(A,B,C,D) = A+B+ A.C.D +A'. C'$$

c) Implement F1 using Look-up Table. Show the content of the Look-Up table.

Question 2

Design the ***fastest circuit*** to implement the following function:

$F = -4X^2$ where X is a 4-bit signed (2's complement) binary number, $X = x_3 x_2 x_1 x_0$

You may use any method that gives optimum delay.
Evaluate your circuit in terms of gate delays and gate counts.

Question 3

Design a 3 bit shift register. The register should shift left to right when x=1 and with x=0 shifts right to left. Assume fill-ins of 0. Start with a state diagram and follow sequential circuit design procedure. Use D Flip Flop for your implementation.

Question 4

a) Design an 8-bit distributed barrel shifter for left to right shifts of up to 6 bits. Assume the shifter is used for arithmetic operations.

b) Multiply the two operands A= -0.75, B= 17.25 using the IEEE 754 floating point multiplication. Show all the required multiplication steps clearly.

Question 5

a. Determine maximum speed of operation at typical conditions for the circuit shown in Fig. 1 below, taking into consideration the fan-out loading only. Timing parameters for all components are listed in Table 1.

b. At the maximum speed of operation, determine the slack time for the setup time and hold time at the T-input of Flip-Flop T.

c. The circuit is implemented on a die which is packaged in a ceramic DIP with a thermal resistance of 30°C/W. Calculate the drop in maximum speed of operation if the die dissipates a power of 2Watts at an ambient temperature of 40°C.

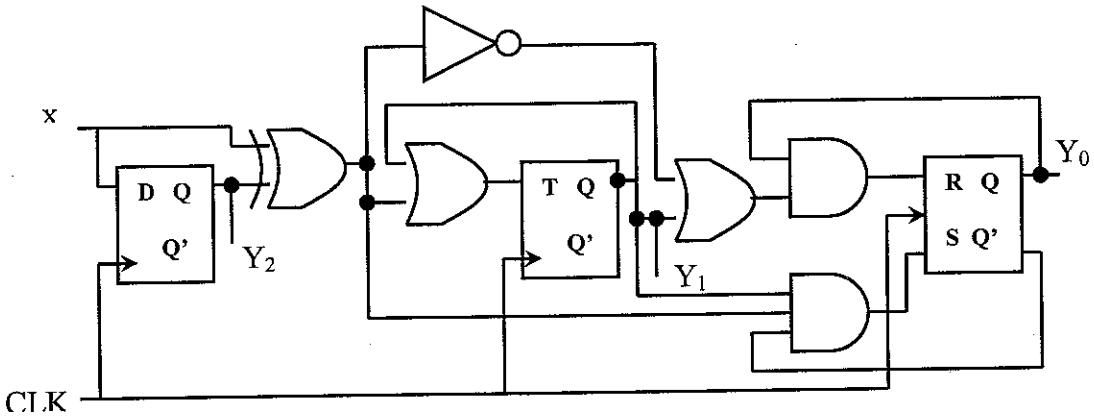


Figure 1

Component	Tp (ns)	Input Loading (UL)	K1 ns/UL
Inverter	**0.15**	**1**	**0.1**
AND/OR(2input)	**0.24**	**2**	**0.05**
XOR (2 input)	**0.4**	**1.5**	**0.12**
Flip Flops, ↑,(CLK to Q) **Tsu=1 ns, t_h = 0.5ns**	**1.5**	**2**	**0.1**

$$Td = \left((Tp + K1\sum Ni + K2\,ML) * K'\right), \quad K' = K_T * K_V * K$$

$$KT = \left(\frac{T2}{T1}\right)1.5, \quad T_J = T_{amb} + \Phi J_a * P_d, \quad K_V = \frac{1}{1+0.01*fv}, \quad K_P = 1+0.01 * f_P$$

Question 6

a) Write a VHDL Code for a 2 to 1 Multiplexer.
The inputs are a, b, and the output is S.

b) There are few errors in the following program. Report the errors:

```
library IEEE;  use ieee.std_logic_1164.all;                    line 1
entity AND_8 is                                                line 2
 port (A,B,C,D,E,F,G,H:in std_logic; Z:out std_logic);          line 3
end AND_8;                                                     line 4
architecture and of AND_8 is                                   line 5
begin Z<=A and B and C and D and E and F and G and H;          line 6
 End and;                                                      line 7
```

c) Draw the circuit given by the VHDL code below. Identify all nodes with their corresponding names clearly.

```
library IEEE;      use ieee.std_logic_1164.all;
entity SUM8 is
   port(carry_in : in std_logic_vector( 7 downto 0 );
      p : in std_logic_vector( 7 downto 0 );
      S : out std_logic_vector( 7 downto 0 ));
end SUM8;
architecture STRUCTURE of SUM8 is
component XOR_2 is
   port ( A, B : in std_logic; Z : out std_logic);
end  component;

begin
   for I in 0 to 7 generate
   B1: block
   for all: XOR_2 use entity WORK.XOR_2(DATA_FLOW);
   begin
      XOR0 : XOR_2 port map(carry_in(I),p(I),s(I));
   end block;
   end generate;
end STRUCTURE;
```

Q1 Final - ~~CDEN 6501~~ Dec 2010

a) Of the several programming technologies in FPGA The following are the most important

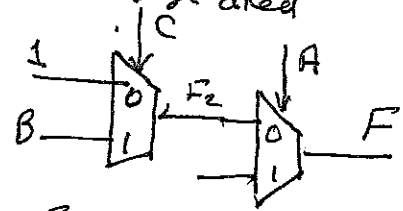
2/10

* SRAM The method is volatile and has high resistance and capacitance it advantages is that it re-programmable in circuit. Consumes power large area
* Antifuse Whether poly to diffusion or metal to metal process has lower resistance and capacitance than the SRAM. The anti fuse is not re-programmable and the process is expensive - small area
* EPROM & EEPROM have higher resistance and capacitance they are non-volatile. There is provision for in circuit programmability for the EEPROM. Consumes power - large area

b)

4/10

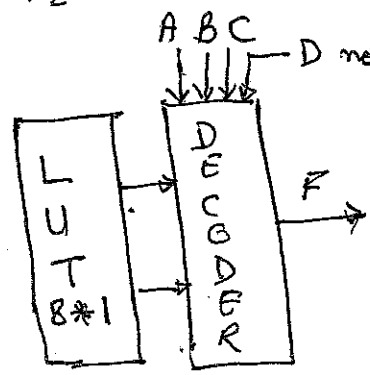
$$F = A + B + A\bar{D} + \bar{A}\bar{C}$$
$$= A + B + \bar{A}\bar{C}$$
$$= A \cdot 1 + \bar{A}\underbrace{(B + \bar{C})}_{F_2}$$

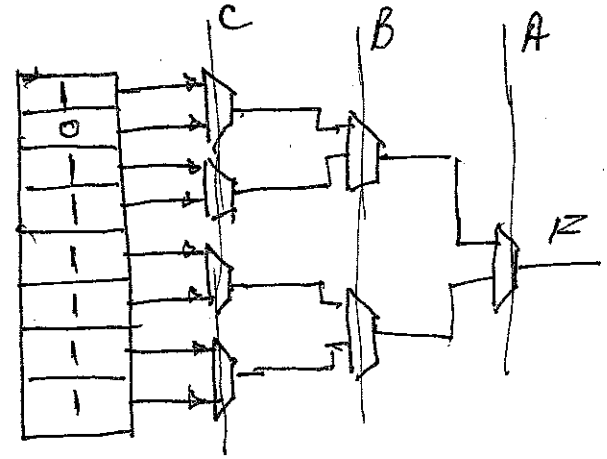


$F_2 = C \cdot B + \bar{C} \cdot 1$

c) 4/10

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1



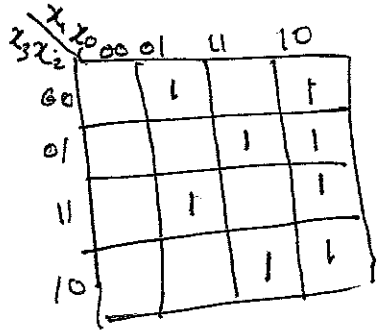


8*1 RAM Cell or Memory Cell

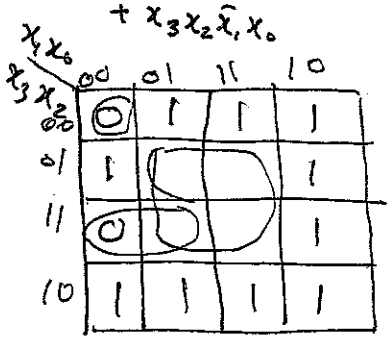
Q2 CEEN6501 Dec 2010

The fastest method in this case would be a 2-level implementation as a SOP

X	x_3	x_2	x_1	x_0	X^2	y_8	y_7	y_6	y_5	y_4	y_3	y_2	y_1	y_0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	1	0	0	0	0	0	0	0	0	1
2	0	0	1	0	4	0	0	0	0	0	0	0	1	0
3	0	0	1	1	9	0	0	0	0	0	0	1	0	1
4	0	1	0	0	16	0	0	0	0	0	1	0	0	0
5	0	1	0	1	25	0	0	0	0	1	1	0	0	1
6	0	1	1	0	36	0	0	0	1	0	0	1	0	0
7	0	1	1	1	49	0	0	0	1	1	0	0	0	1
-8	1	0	0	0	64	0	0	1	0	0	0	0	0	0
-7	1	0	0	1	49	0	0	0	1	1	0	0	0	1
-6	1	0	1	0	36	0	0	0	1	0	0	1	0	0
-5	1	0	1	1	25	0	0	0	0	1	1	0	0	1
-4	1	1	0	0	16	0	0	0	0	1	0	0	0	0
-3	1	1	0	1	9	0	0	0	0	1	0	0	1	1
-2	1	1	1	0	4	0	0	0	0	1	1	0	0	0
-1	1	1	1	1	1	0	0	0	0	1	1	1	0	1

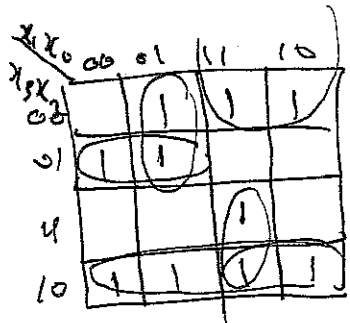


$f_5 = x_1\bar{x}_0 + x_1\bar{x}_3x_2 + x_3\bar{x}_2x_1 + \bar{x}_3\bar{x}_2\bar{x}_1x_0 + x_3x_2\bar{x}_1x_0$



$f_6 = (\bar{x}_2 + x_0)(\bar{x}_3 + \bar{x}_2 + x_1)(x_3 + x_2 + x_1 + x_0)$

$F = -4X^2 = f_8 f_7 f_6 f_5 f_4 f_3 f_2 f_1 f_0$



$f_7 = \bar{x}_2x_1 + x_3\bar{x}_2 + \bar{x}_3\bar{x}_1x_0 + \bar{x}_3x_2x_1 + x_3x_1x_0$

2 level implementation

$f_0 = 0$

$f_1 = 0$

$f_2 = x_0$

$f_3 = x_0$

$f_4 = x_0 + x_1$

$f_5 = x_1x_0 + x_0\bar{x}_1\bar{x}_2\bar{x}_3 + x_0x_1x_2\bar{x}_3 + x_0\bar{x}_1x_2x_3 + x_0x_1\bar{x}_2x_3$

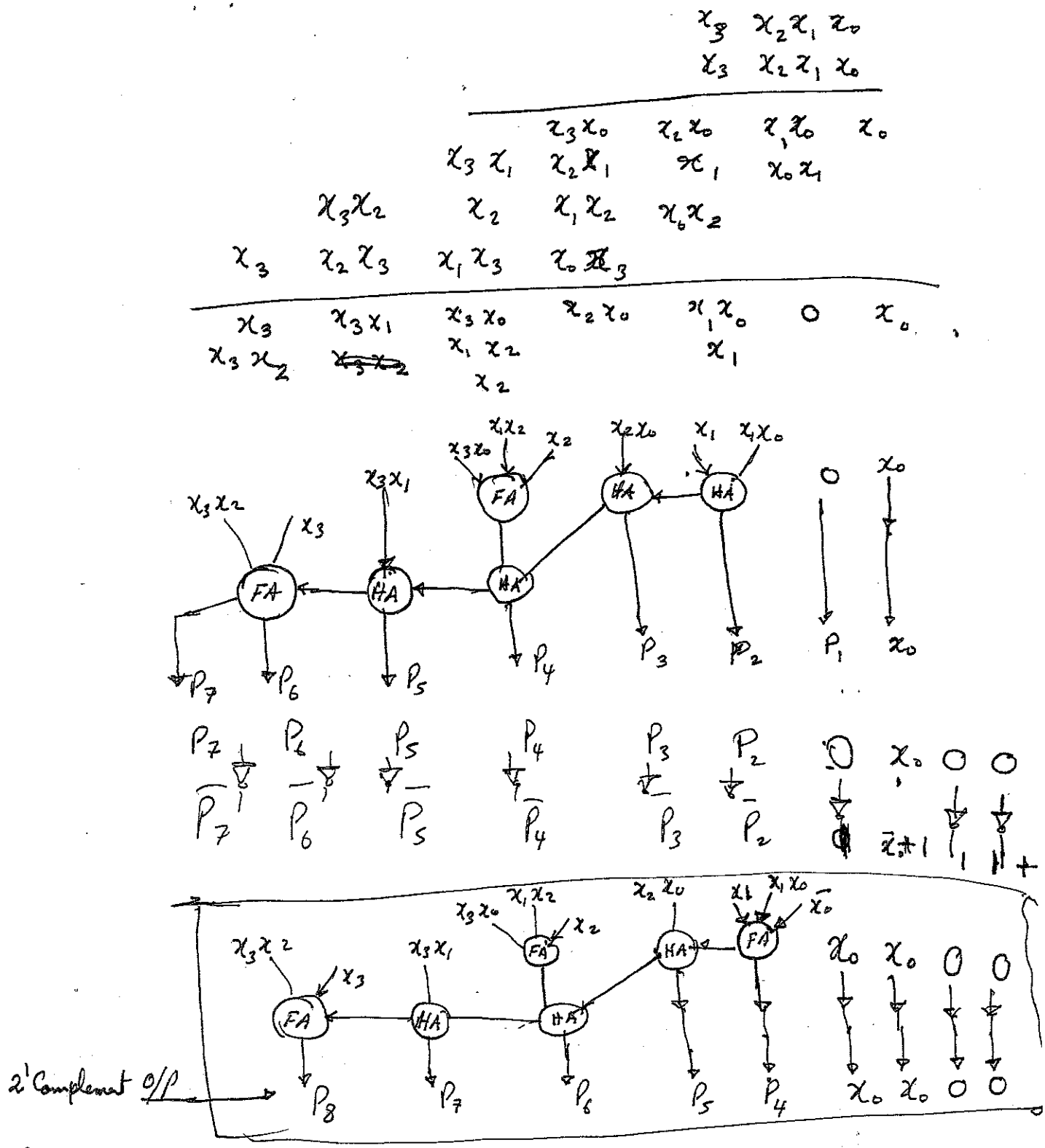
$f_6 = x_1\bar{x}_0 + x_3\bar{x}_2 + \bar{x}_2x_0 + \bar{x}_0x_2\bar{x}_3$

$f_7 = \bar{x}_2x_1 + x_3\bar{x}_2 + x_0\bar{x}_1\bar{x}_3 + x_2\bar{x}_3\bar{x}_1 + x_3x_1x_0$

$f_8 = x_3 + x_2 \mp x_1 + x_0$

2's Complement o/p

Q2 Alternative if we assume X is unsigned number

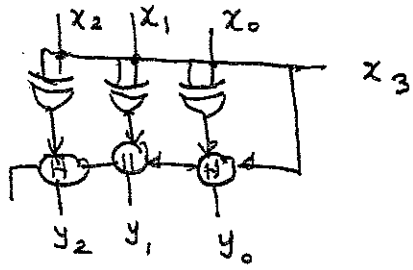


Please note that $\bar{x}_0 + 1 = x_0$ with a carry of $\bar{x}_0$.

Area of 3 FA + 3 HA + 9 inverters

delay is $2\gamma_{FA} + 3\gamma_{HA}$

Q2 signed number



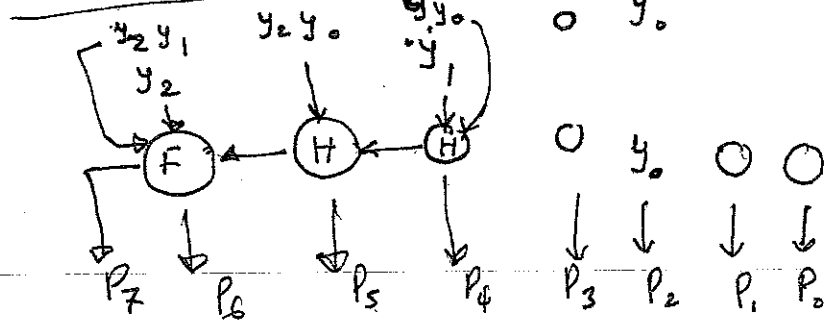
$y_2\ y_1\ y_0$

$y_2\ y_1\ y_0$

$y_2 y_0$ $y_1 y_0$ $y_0 y_0$

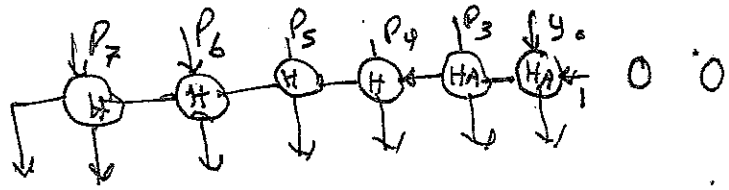
$y_2 y_1$ $y_1 y_1$ $y_0 y_1$

$y_1 y_2$ $y_1 y_2$ $y_0 y_2$



4 x X

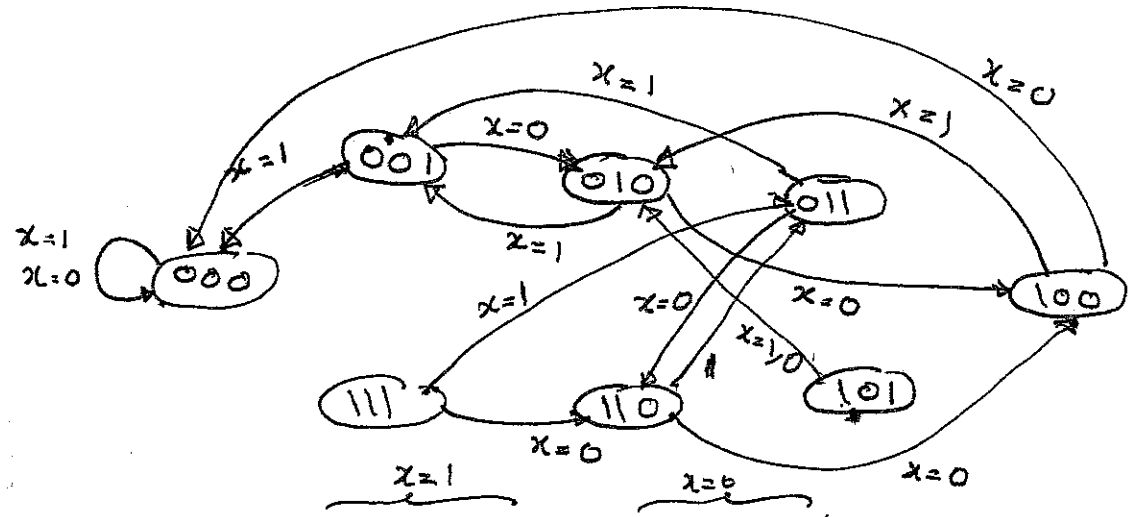
now to get - 4 X we take 2's Complent of this Values



Q3

3-bit left-right shift will have $2^3 = 8$ states

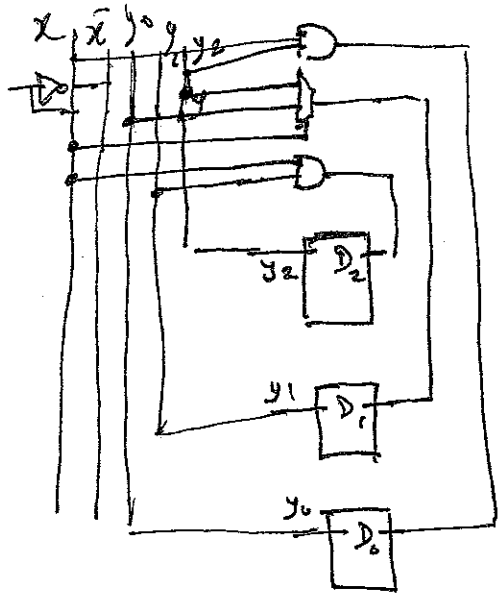
$x=1$ L → R
$x=0$ R → L



y_0	y_1	y_2	$x=1$: y_0^+	y_1^+	y_2^+	$x=0$: y_0^+	y_1^+	y_2^+
0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	1	0
0	1	0	0	0	1	1	0	0
0	1	1	0	0	1	1	1	0
1	0	0	0	1	0	0	0	0
1	0	1	0	1	0	0	1	0
1	1	0	0	1	1	1	0	0
1	1	1	0	1	1	1	1	0

Reading directly from the Table

$$y_2^+ = x y_1 \quad = D_2^+$$
$$y_1^+ = \bar{x} y_2 + x y_0 \quad = D_1^+$$
$$y_0^+ = \bar{x} y_1 \quad = D_0^+$$



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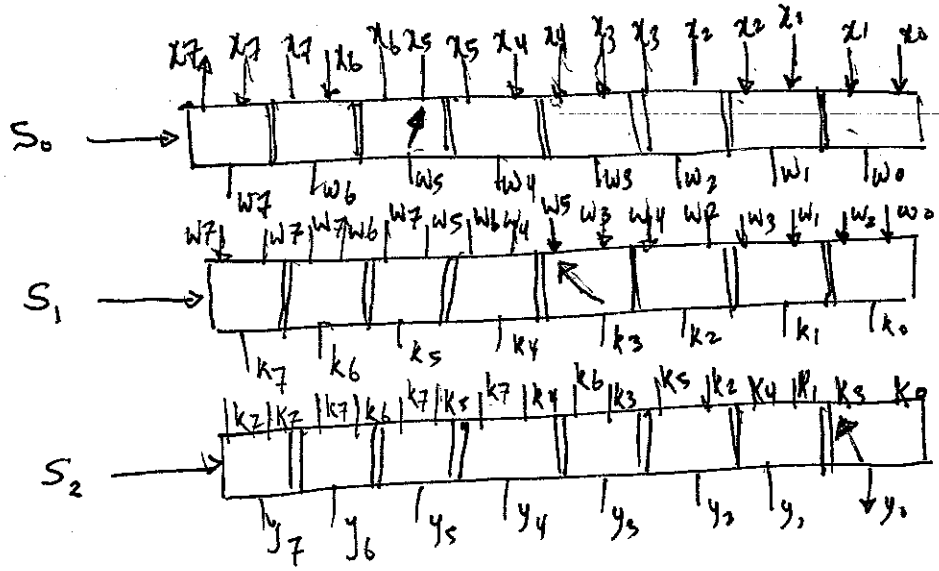

b)

$A = -0.75$
$= -0.1 * 2^{-1}$
$e_A = 127 - 1 = 126$

$A =$ | 1 | 0111 1110 | 1000 → 0 |
1 8 23

$B = 17.25$
$= 10001.01$
$e_B = 127 + 4 = 131$

| 0 | 1000 0011 | 0001010 |
1 8 23

$Sign = S_A \oplus S_B = 0 \oplus 1 = 1$

Exponent
$$\begin{array}{r} 0111\ 1110 \\ +\ 1000\ 0011 \\ \hline 01000\ 0001 \\ -127\ (1000\ 0001) \\ \hline 01000\ 0010 \end{array}$$

multiplication
$$\begin{array}{r} 1.000101 \\ 1.1\ * \\ \hline 1000101 \\ 1000101 \\ \hline 1.1400\ 11\ 11 \end{array}$$

normalize
$1.100\ 1111 * 2^{D}$

final Mantena $M = 100\,1111$
" Exponent $e_R = 1000\ 0010$

No rounding necessary

Pad results

| 1 | 1000 0010 | 100 1111000 → |
1 8 23

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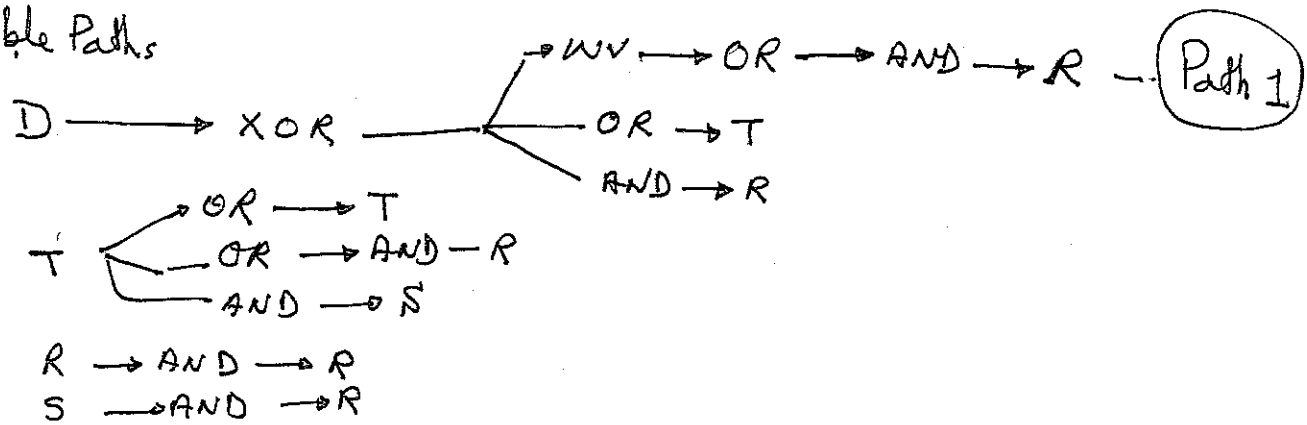
Possible Paths



Since all FFs have the same loading & fan-out the Path 1 is the critical Path

$$T_{CL_{max}} = \underbrace{0.1 * 1.5}_{D,FF} + \underbrace{0.4 + 0.12(2+2+1)}_{XOR} + \underbrace{0.15 + 0.1(2)}_{INV} +$$

$$\underbrace{0.24 + 0.05(2)}_{OR} + 0.24 + 0.05(2) = 2.18 \text{ ns}$$

$$T = \underbrace{1.5}_{t_{CQ}} + \underbrace{2.18}_{t_{CL\,max}} + \underbrace{1}_{t_{su}} = 4.68 \quad \text{Max Speed} = 213 \text{ MHz}$$

Having obtained The maximum T for the whole circuit we now focus on FF, T to determine the slack in set up time and hold time

P_2 Longest Path D → XOR − OR → T

P_3 Shortest Path T → OR → T

$$T_{P_2} = \underbrace{0.1 * 1.5}_{D,FF} + \underbrace{0.4 + 0.12(2+2+1)}_{XOR} + \underbrace{0.24 + 0.05 \times 2}_{OR}$$

$$= 1.49 \text{ ns}$$

$$T_{path_2} = 1.49 + 1.5 + 1 = 3.99$$

$$T_{set\,up\ slack} = T_{max} - T_{P_{2\,max}} = 4.68 - 3.99 = 0.69 \text{ ns}$$

$$T_{P_{3\,min}} = \underbrace{0.1(2+2+2)}_{T_{FF}} + \underbrace{0.24 + 0.05 \times 2}_{OR} = 0.94$$

$$T_{T_{min}} = 1.5 + 0.94 = 2.44$$

Hold Slack = 2.44 − 1.92 = 1.92 ns

Q5 COEN 6501 Dec 2010

$$K_T = \left(\frac{T_2}{T_1}\right)^{1.5} = \left(\frac{273 + 40 + 30*2}{273 + 40}\right)^{1.5} = 1.3$$

$$\text{New Speed} = \frac{\text{Max Speed}}{K_T} = 163 \text{ MHz}$$

Q6 CEEN6501 Dec 2010

a) 2 → 1 MUX

```
library ceee;
use ieee.std_logic_1164.all;
entity MUX is
    port (a, b, c: in std_logic; s: out std_logic);
end MUX
architecture behavioral of MUX is
begin
    s <= (a and c) or (b and not c);
end behavioral;
```

(or a as bit_vector(et))

b

line 2: missing "is"
line 3: " ";" and ")"
line 4: "s" undefined
line 5: "and" is a reserved word
line 6: "begin" missing
line 7: "and" is a reserved word

} 6 errors

c –