**Digital Design COEN 6501 Midterm exam. Oct 17th , 2016**

**Answer all questions. Time allowed 1 hr 30 min.**

**All questions carry equal mark A. J. Al-Khalili.**

**Question 1:**

Using array multipliers give an ***optimum*** circuit for calculation of Y:

Y= [4 **N( N )** ] **-** 1

where N is a 3-bit unsigned binary number. N = a2 a1 a0

Show your implementation with **N = 2.**

Give a detailed estimate of delay and area (Full Adder, Half Adder AND gate or other entity used).

Show the input to each adder clearly.

**Question 2:**

You are to design a 9 bit adder. You have two choices to design the adder: either a Carry Ripple Adder or a Carry Select Adder. Your design Criterion is (A.T, The area time product) where A, is the Area and T is the time delay. You are given the following parameters:

Full Adder Delay= TFA  Full Adder Area = AFA

MUX Delay = ½ TFA  MUX Area = 1/3 AFA

Give your optimum Design.

**Question 3:**

Multiply The following floating point numbers A \* B

A = 21.7510 B = **-**7.2510

Give your final result in a packed format. Use IEEE 754 format.