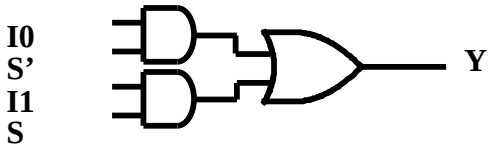
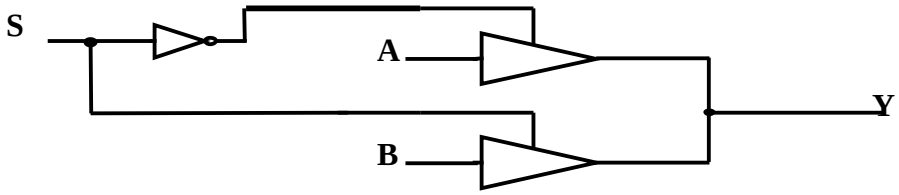
EE 3714 Test #3 Solutions- Spring 2000 – Reese

Work all problems.

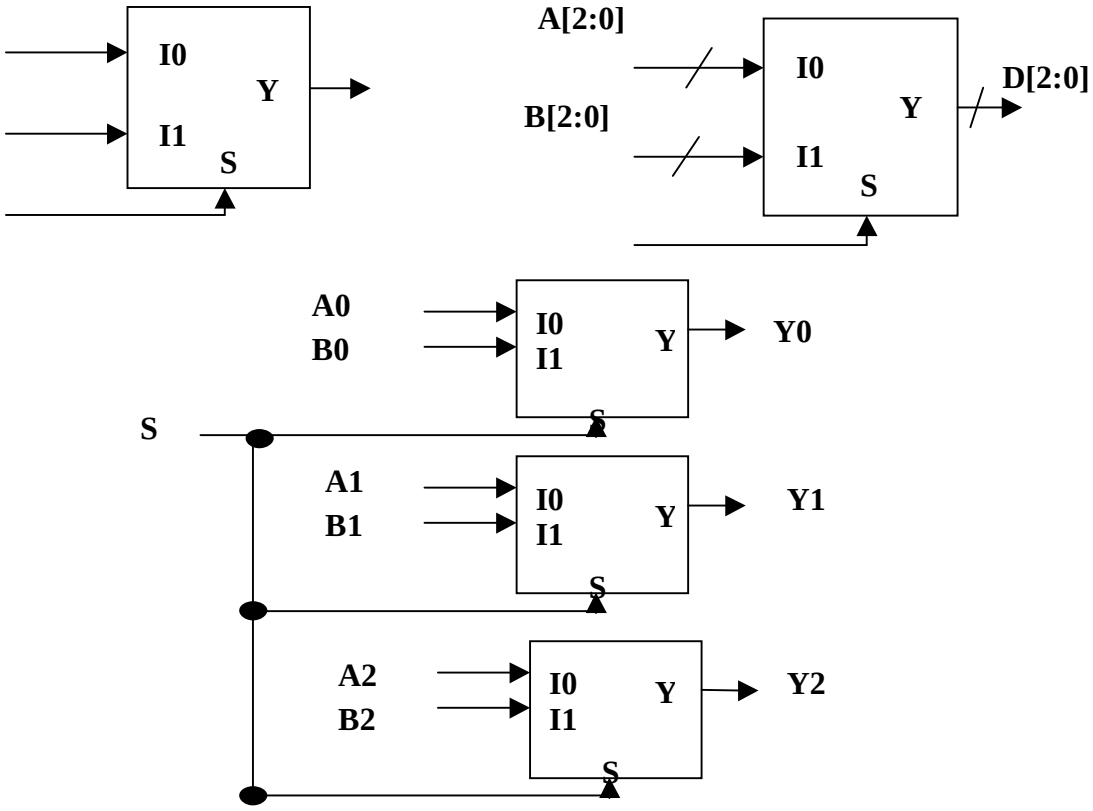
1. (6 pts) Draw the schematic of a 2/1 mux using only combinational gates.



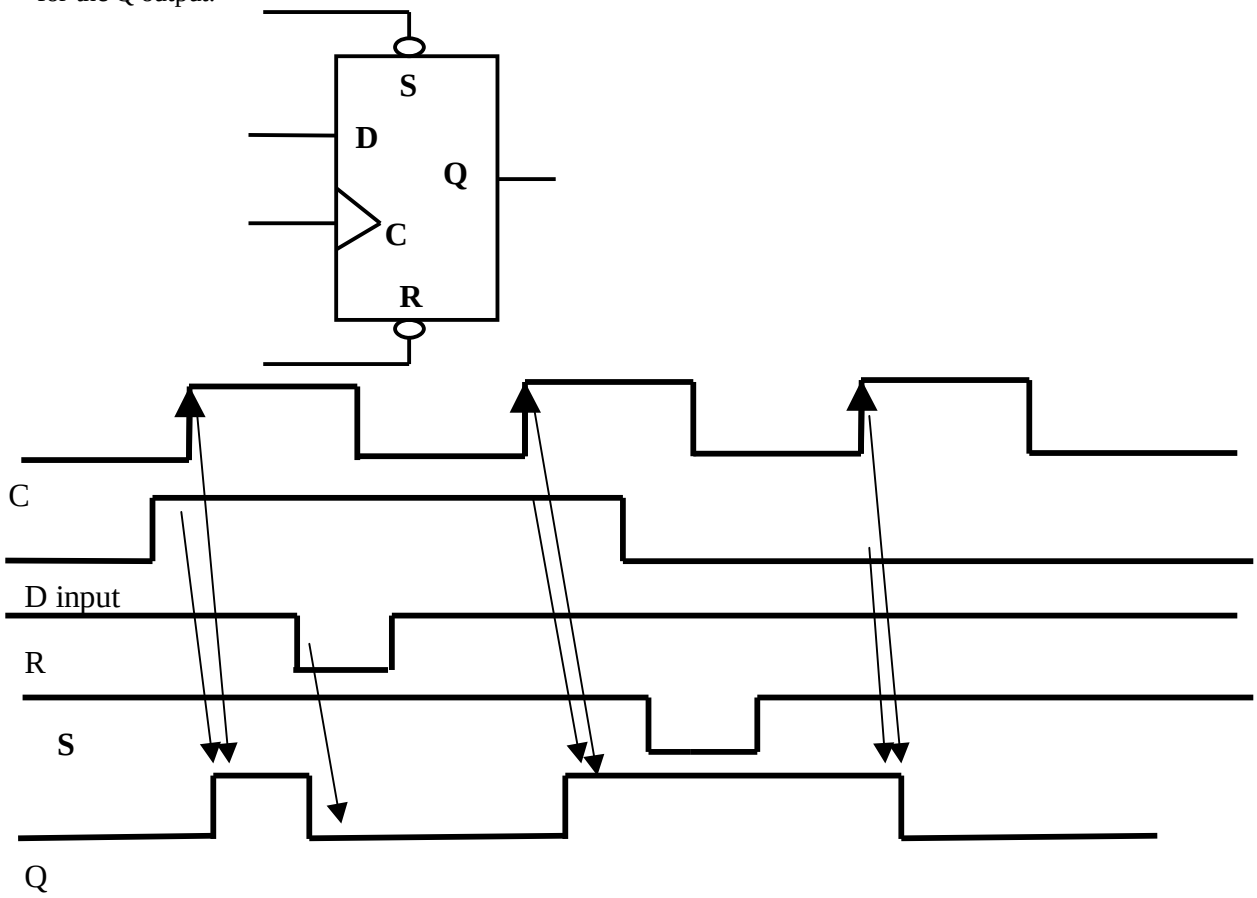
2. (6 pts) Draw the schematic of a 2/1 mux using tri-state buffers plus combinational gates.



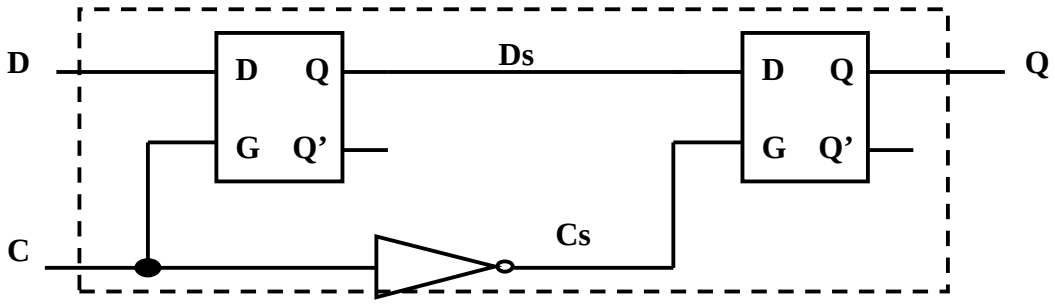
3. (8 pts) The symbol on the left is for a one-bit 2/1 mux. The symbol on the right is for a three bit 2/1 mux. Draw a schematic showing how to create the three bit 2/1 mux using the one-bit 2/1 mux.



4. (8 pts)Assume that the initial state device shown below is a '0'. Complete the timing diagram below for the Q output.

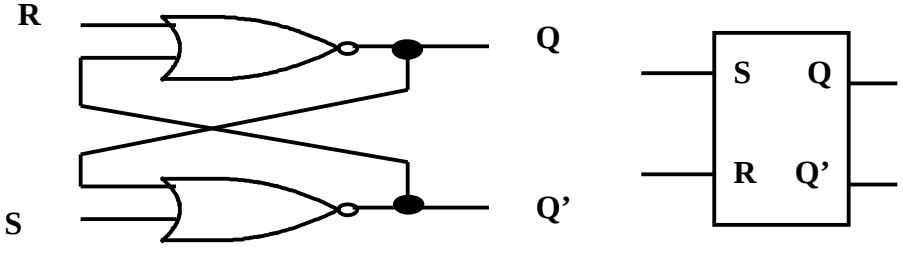


5. (8 pts) Draw the schematic for a falling edge-triggered D-FF using D latches.

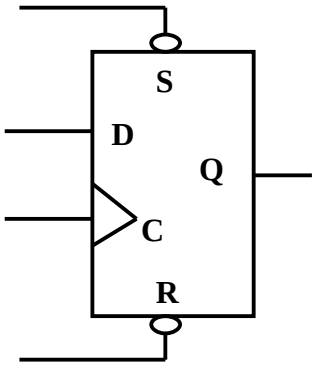


6. (8 pts) Draw the gate level schematic for an SR latch, either with high true inputs or low true inputs. Indicate if your SR inputs are high or low true. (you will not get credit if you indicate that you have an SR with low true inputs, yet your gate level implementation is for high true inputs, or vice-versa).

high true inputs



7. (8 pts) For the device shown below, indicate what type of TIMINGS might be found in the datasheet for the following inputs (circle ONE OR MORE timing for each input).



Correct Choices shown in **BOLD**.

a. D input	TPLH	TPHL	**Setup**	**Hold**
b. C input	**TPLH**	**TPHL**	Setup	Hold
c. S input	**TPLH**	TPHL	Setup	Hold
d. R input	TPLH	**TPHL**	Setup	Hold

D input only has setup/hold, no prop delay because it is clock edge that triggers change on Q output, not change on D input. C input can cause Q to go to either '1' or '0', so has both TPLH and TPHL. S input can only change Q to 1, so only TPLH. R input can only cause Q to go to '0', so only TPHL.

8. (5 pts) Given a clock period of 5 ns, what is the clock FREQUENCY in MHz!!!!!!

Freq = $1/(5 \times 10^{-9}) = 0.2 \times 10^{9} = 200 \times 10^{6} = 200$ MHz

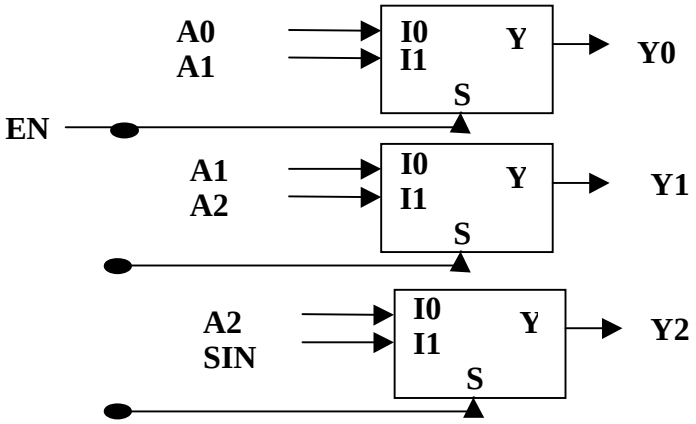
9. (5 pts) What is the value of $54 shifted to the LEFT by one position with the serial input bit = '1'?

$54 = 0 1 0 1 0 1 0 0 SIN(1)

left shift 1 0 1 0 1 0 0 1 = $A9

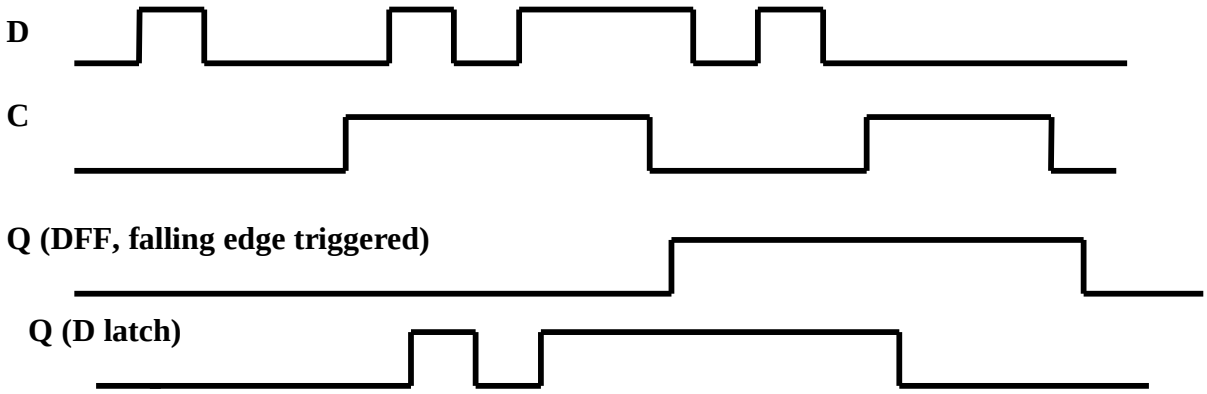
10. (10 pts)Draw the schematic for a 3 bit RIGHT shift combinational logic block built using 2/1 muxes. The 3 bit left shifter will do the following:

When EN = 0, Y[2:0] = A[2:0]
When EN = 1, Y = A RIGHT shifted by 1, serial input bit is 'SIN'.



Y2Y1Y0 = A2A1A0 when EN=0
Y2Y1Y0 = SINA2A1 when EN=1

11. (8 pts) Illustrate via a timing diagram the DIFFERENCE between a D-latch and a D-FF.



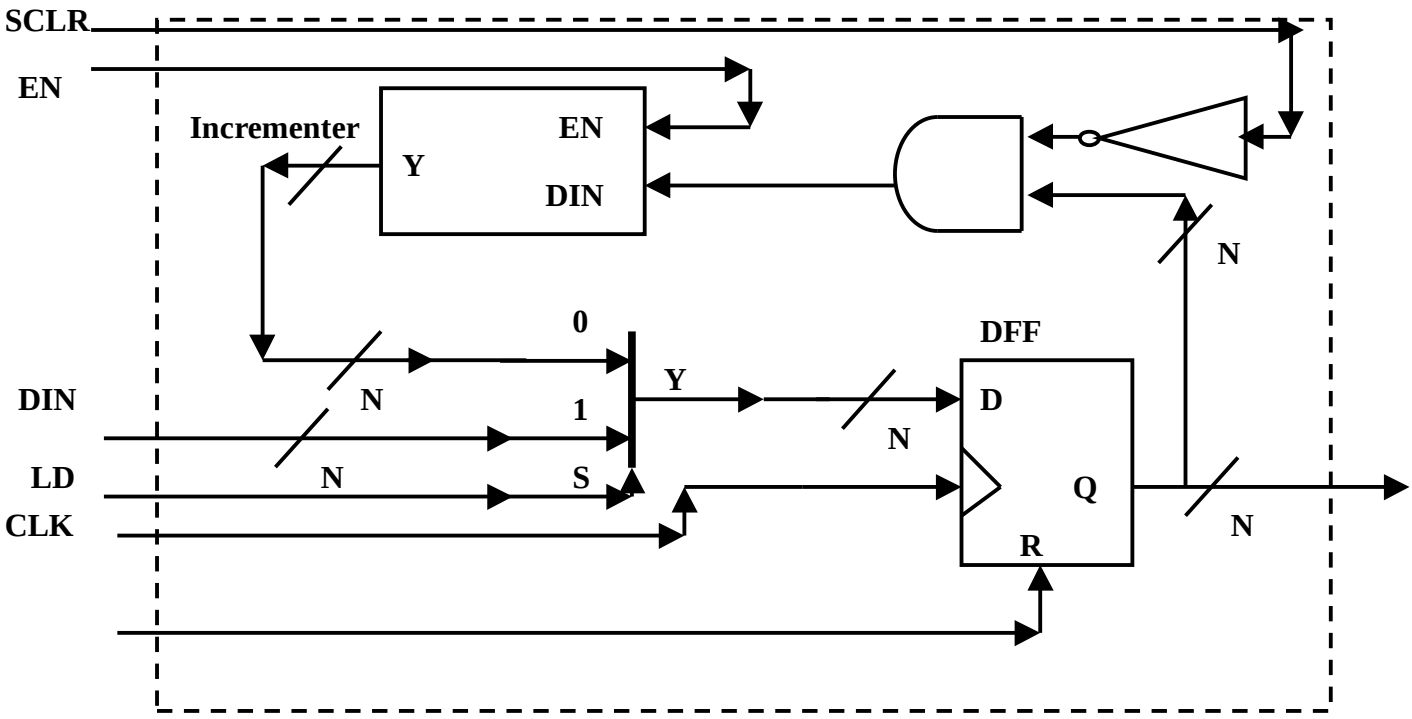
12. (5 pts) Fill in the following truth table for a J-K FF (rising-edge triggered)

CLK	J	K	PS (Q)	NS (Q+)
↑	0	0	Q	Q (hold)
↑	0	1	Q	0 (reset)
↑	1	0	Q	1 (set)
↑	1	1	Q	Q' (toggle)

13. (5 pts) Fill in the following truth table for a Toggle (T) FF (rising-edge triggered)

CLK	T	PS (Q)	NS (Q+)
↑	0	Q	Q (hold)
↑	1	Q	Q' (toggle)

14. (10 pts) The schematic below shows a count-up counter with a load and synchronous clear capability.



The following table lists all 8 combinations of the three control lines: LD, EN, SCLR. Besides each combination of LD, EN, SCLR, describe what the new value of the counter will be:

a. KEEP old value
b. INC old value by 1
c. DIN (load din)
d. DIN + 1 (load DIN + 1)
e. 0 (clear register)
f. 1 (load a '1' into register)

Put something for EVERY combination.

LD	EN	SCLR	ACTION
0	0	0	Keep Old Value
0	0	1	0 (clear register)
0	1	0	INC old vlaue by 1
0	1	1	1 (load a '1' into register)
1	0	0	DIN (load din)
1	0	1	DIN (load din)
1	1	0	DIN (load din)
1	1	1	DIN (load din)