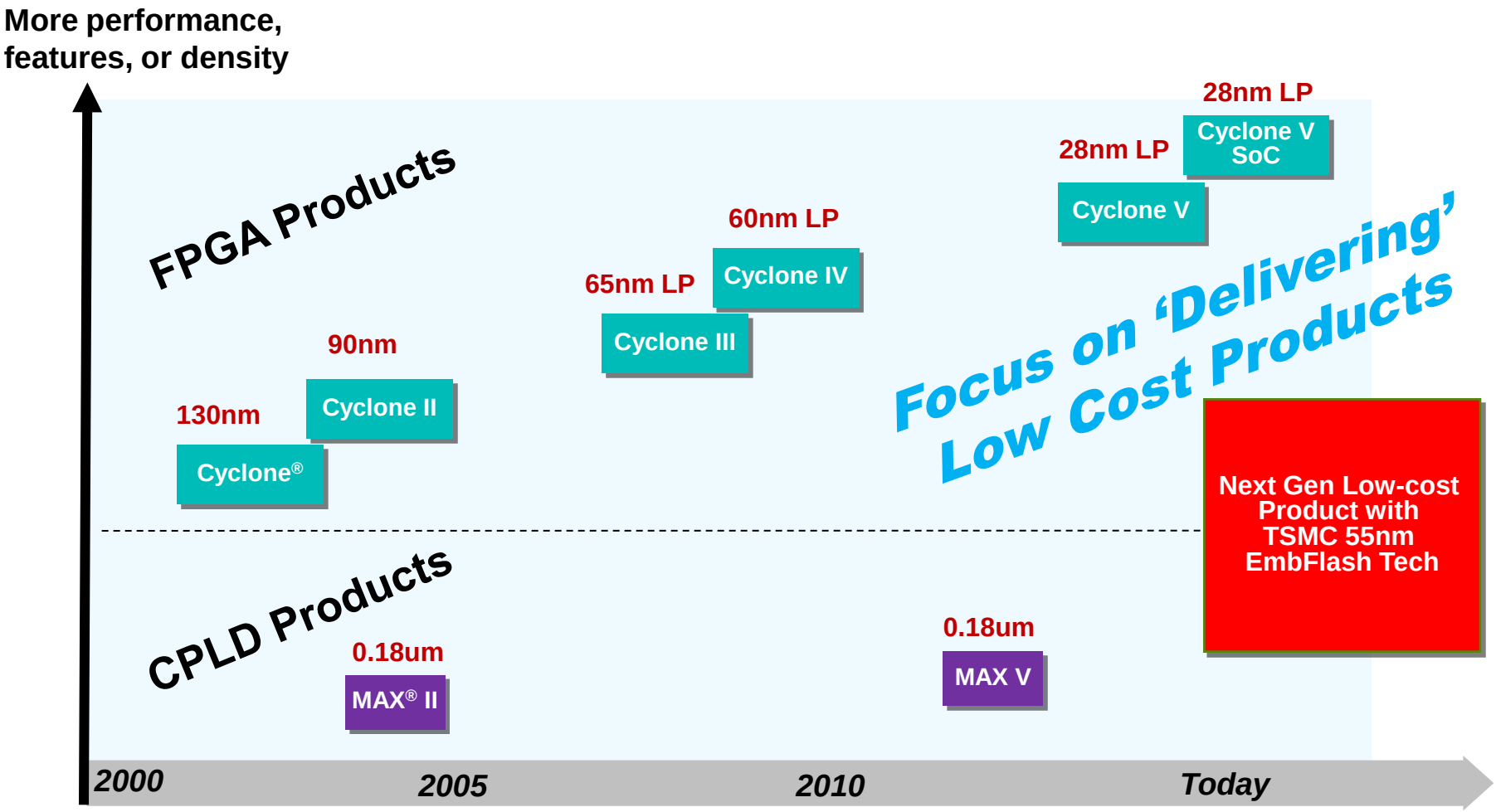
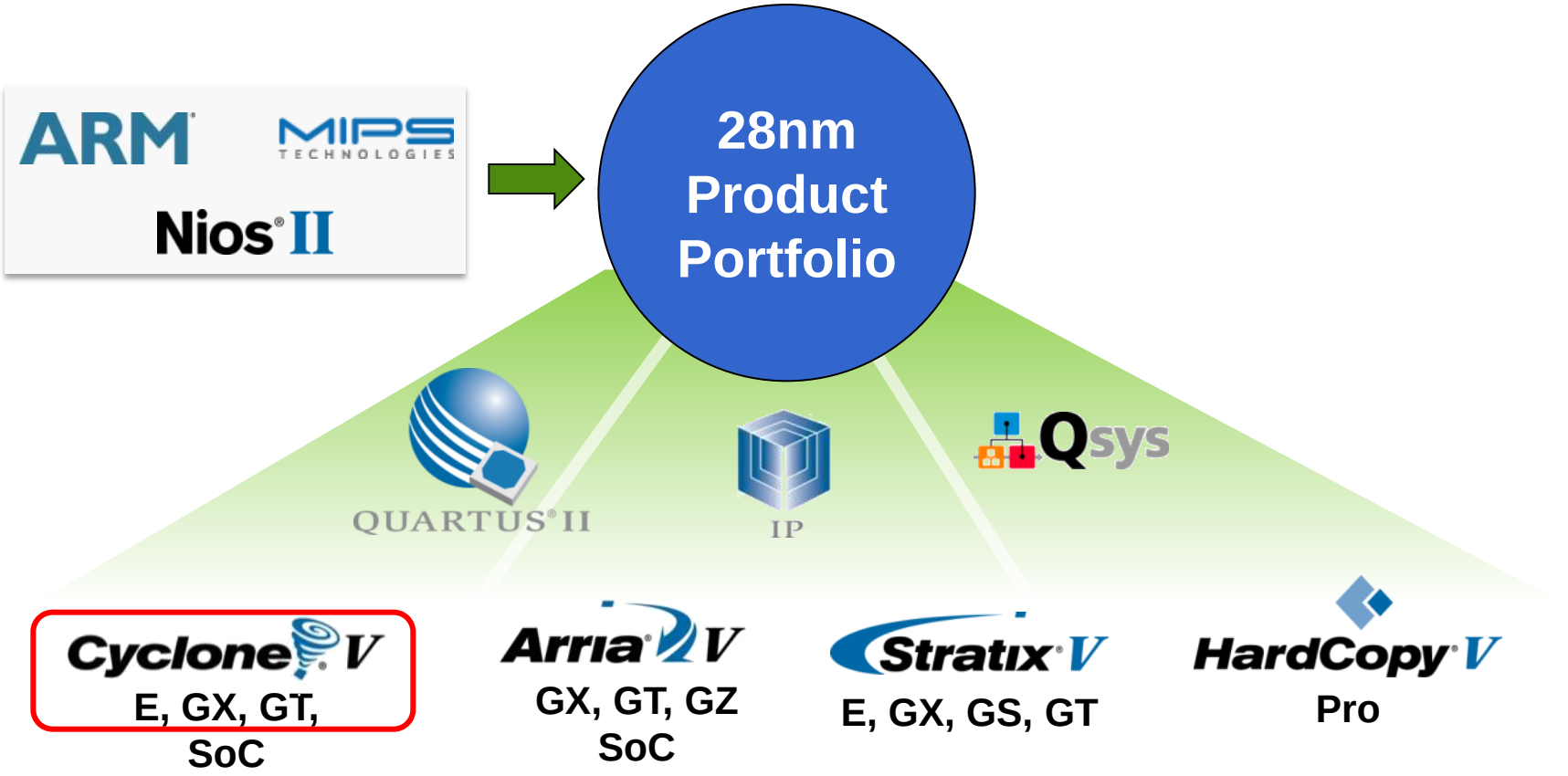
Ease Your Life
With Altera Low-Cost Products

AP Technology Roadshow 2013

Low Cost Product Families – Rollout History



Broadest 28nm Product Portfolio



More Products Than Any Other Prior Node

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28HP & 28LP are Industry Processes of Choice

Vendors using 28HP & 28LP

ALTERA

QUALCOMM

Source: Semiconductor Manufacturing and Design

AMD

28nm GPU at TSMC source: Taiwan Economic News

NETLOGIC MICROSYSTEMS

Source: Netlogic Micro and Magma

Moortec semiconductor

analogue IP · custom chip · platforms

Source: Power Systems Design

NVIDIA

28nm GPU at TSMC source: Digitimes

Vendors using 28HPL

XILINX

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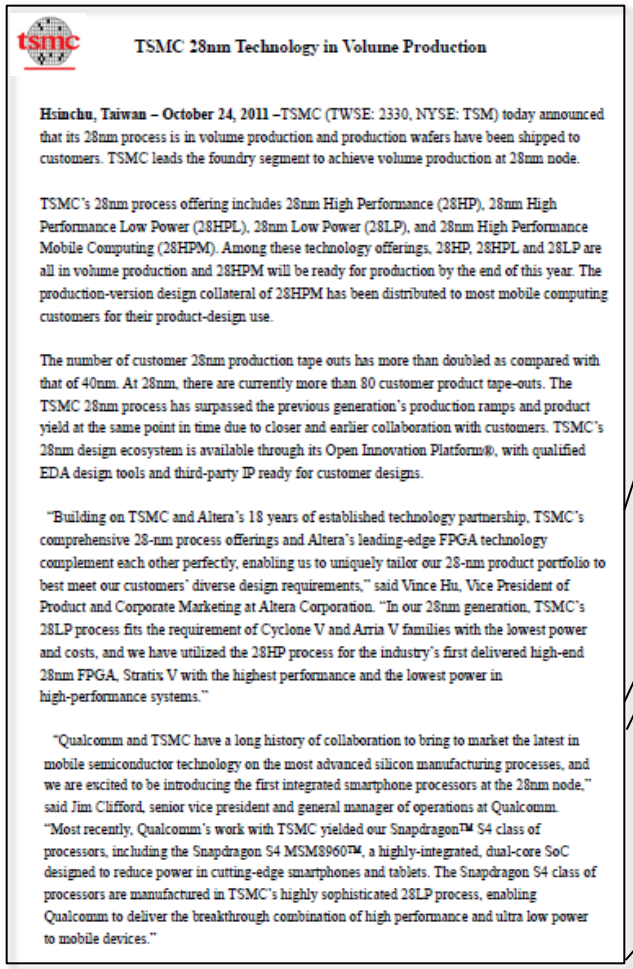
Major Semiconductor Vendors Choose TSMC's 28LP Process for Lowest Power



TSMC 28nm Technology in Volume Production

Hsinchu, Taiwan – October 24, 2011 –TSMC (TWSE: 2330, NYSE: TSM) today announced that its 28nm process is in volume production and production wafers have been shipped to customers. TSMC leads the foundry segment to achieve volume production at 28nm node.

TSMC's 28nm process offering includes 28nm High Performance (28HP), 28nm High Performance Low Power (28HPL), 28nm Low Power (28LP), and 28nm High Performance Mobile Computing (28HPM). Among these technology offerings, 28HP, 28HPL and 28LP are all in volume production and 28HPM will be ready for production by the end of this year. The production-version design collateral of 28HPM has been distributed to most mobile computing customers for their product-design use.

The number of customer 28nm production tape outs has more than doubled as compared with that of 40nm. At 28nm, there are currently more than 80 customer product tape-outs. The TSMC 28nm process has surpassed the previous generation's production ramps and product yield at the same point in time due to closer and earlier collaboration with customers. TSMC's 28nm design ecosystem is available through its Open Innovation Platform®, with qualified EDA design tools and third-party IP ready for customer designs.

"Building on TSMC and Altera's 18 years of established technology partnership, TSMC's comprehensive 28-nm process offerings and Altera's leading-edge FPGA technology complement each other perfectly, enabling us to uniquely tailor our 28-nm product portfolio to best meet our customers' diverse design requirements," said Vince Hu, Vice President of Product and Corporate Marketing at Altera Corporation. "In our 28nm generation, TSMC's 28LP process fits the requirement of Cyclone V and Arria V families with the lowest power and costs, and we have utilized the 28HP process for the industry's first delivered high-end 28nm FPGA, Stratix V with the highest performance and the lowest power in high-performance systems."

"Qualcomm and TSMC have a long history of collaboration to bring to market the latest in mobile semiconductor technology on the most advanced silicon manufacturing processes, and we are excited to be introducing the first integrated smartphone processors at the 28nm node," said Jim Clifford, senior vice president and general manager of operations at Qualcomm. "Most recently, Qualcomm's work with TSMC yielded our Snapdragon™ S4 class of processors, including the Snapdragon S4 MSM8960™, a highly-integrated, dual-core SoC designed to reduce power in cutting-edge smartphones and tablets. The Snapdragon S4 class of processors are manufactured in TSMC's highly sophisticated 28LP process, enabling Qualcomm to deliver the breakthrough combination of high performance and ultra low power to mobile devices."

[Click here for full press release]

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TSMC 28LP: Qualcomm's process choice to deliver lowest power for mobile devices

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Cyclone V FPGAs

Cyclone V FPGAs: Lowest System Cost and Power

- **Lowest system cost**
  - Only two required voltage rails for simple power distribution
  - Partial reconfiguration
  - Configuration via Protocol (CvP)
  - Wire bond packaging
  - Hardened IP to save time and cost
    - Memory controller for DDR3, DDR2, LPDDR2
    - PCIe Gen 1 and 2
    - Variable Precision DSP blocks
    - PLLs with 32 bit fractional frequency synthesis
- **Lowest system power**
  - 40% lower total power than previous generation
  - Lowest transceiver power at any data rate
  - 28-nm LP process for the lowest static power
- **Maximum Functionality**
  - 300K logic elements
  - 11.6 Mbits of block memory
  - Up to 342 variable precision DSP blocks
  - Up to 560 User IO
  - Up to 2 PCIe blocks
  - Up to 2 hardened memory controller blocks
  - Up to 12 x 5G transceivers

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Cyclone V FPGA Family

Opening Up Design Possibilities

	Lowest cost and power	3G transceivers	5G transceivers
	*Optimized for lowest system cost and power for a wide spectrum of general logic and DSP applications*	*Optimized for lowest cost and power for 614 Mbps to 3.125 Gbps transceiver applications*	*FPGA industry's lowest cost and power for 5.0 Gbps transceiver applications*
FPGA	**E Variant**	**GX Variant**	**GT Variant**
Integrated ARM Cortex-A9 MPCore Processor System	**SE Variant**	**SX Variant**	**ST Variant**

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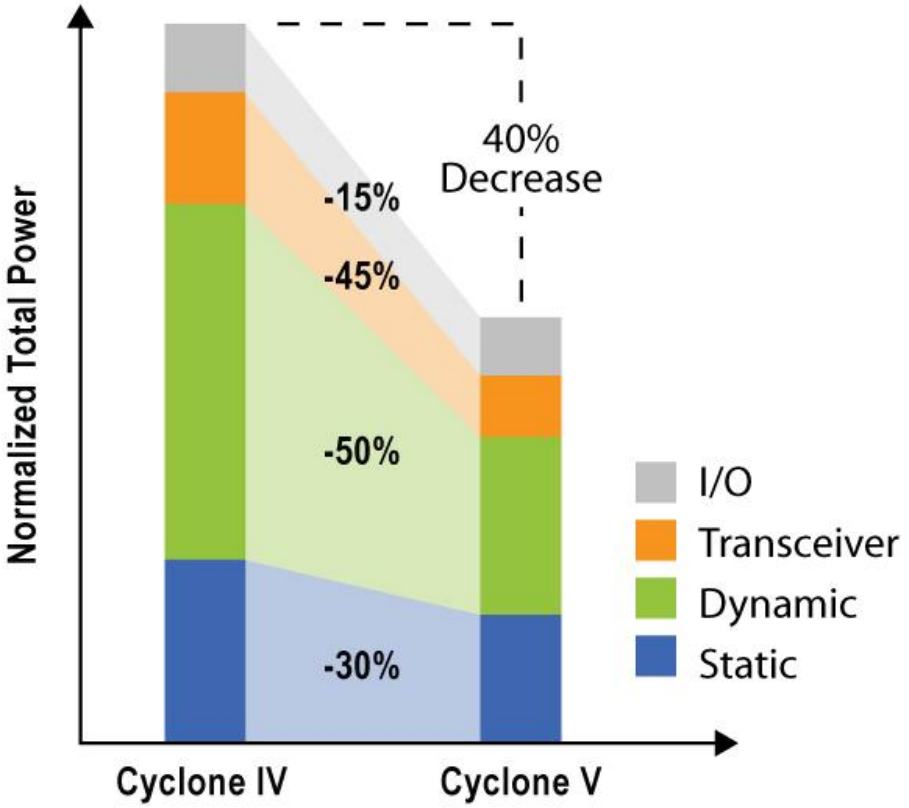
Cyclone V FPGAs Reduce Power Up to 40%

28-nm LP benefits:

- Lower capacitance
- Multi-threshold transistors
- Variable channel lengths reduce leakage
- Reduced core voltage



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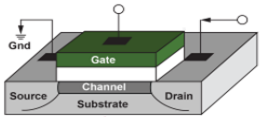
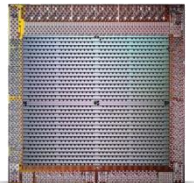
Cyclone V FPGAs: Designed for Low Power



28LP Process

- Lower capacitance
- Multi-threshold
  ...sistors



Low-Power Device Architecture

- Hard memory controller
- Hard PCIe Gen2
- Low-power transceivers
- Thermal efficient package design

Largest Power Savings by Device Architecture

Up to 40% Power Savings

QUARTUS II

Power-Aware Design Tools

- Push-button power optimization

Relative Total Power

1.0

0.6

15%

25%

10% Average Reduction in Dynamic Power

Cyclone IV FPGAs (60nm LP process)

28LP Process and IC Optimization

Low-Power Architecture

Software Optimization

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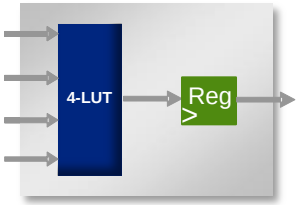
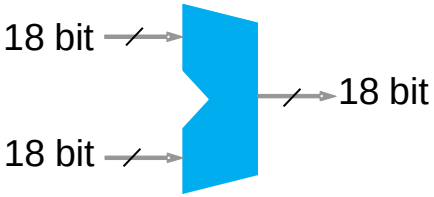
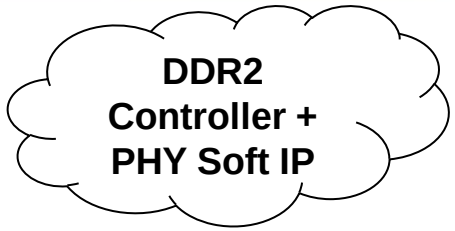
Cyclone V: Innovations in Leaps and Bounds

Cyclone IV FPGAs

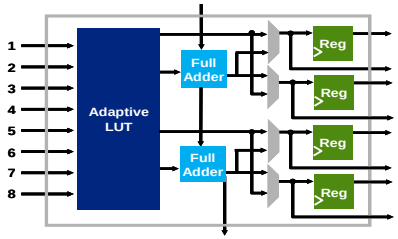


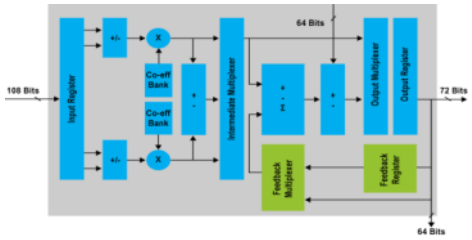


M9K



Cyclone V FPGAs

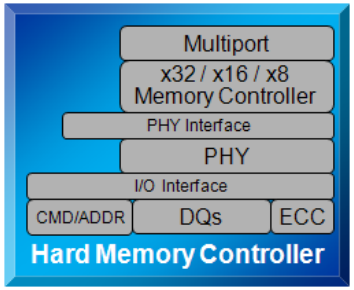




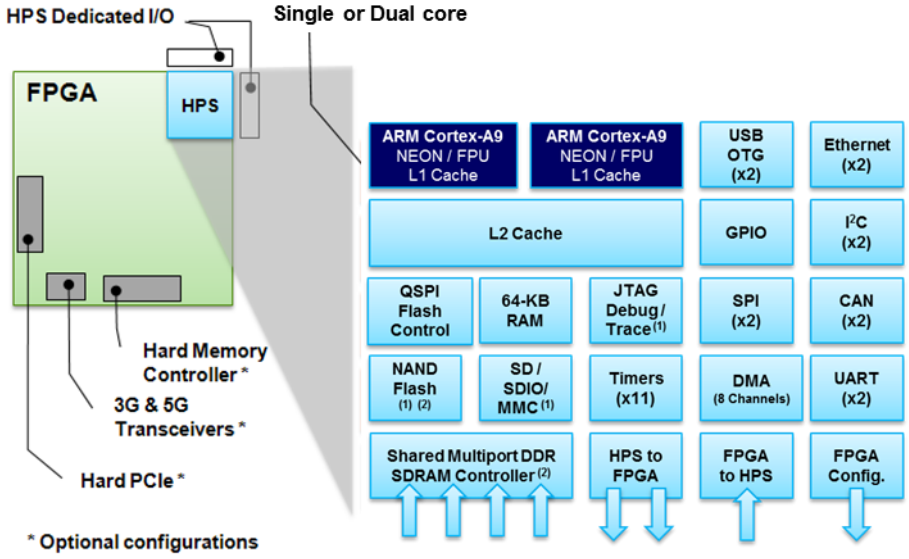
M10K

MLAB

640 bits



Cyclone V SoC FPGAs



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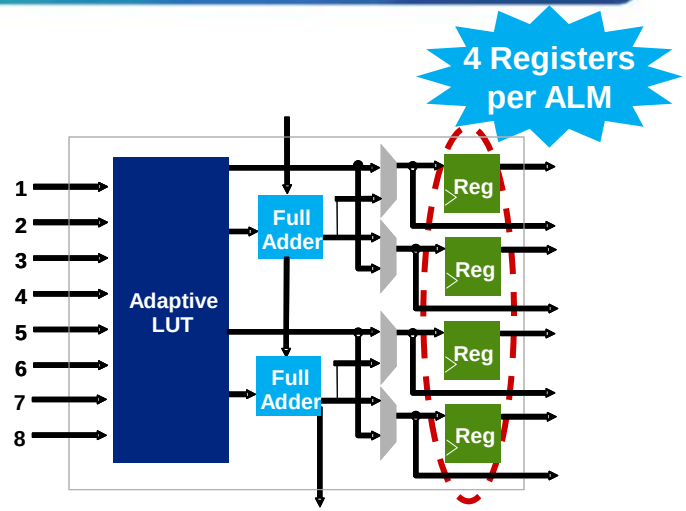
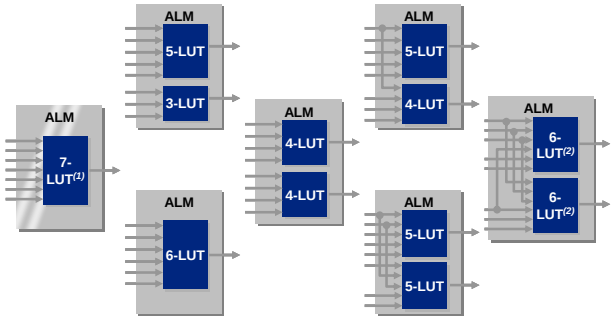
Adaptive Logic Module (ALM)

- **Improves logic efficiency vs. 4-LUT module**
  - 8-input fracturable look-up table (LUT) efficiency
  - 1 ALM = 2.65 LEs
  - Four registers improve timing closure for register-rich or heavily pipelined designs



- **Optimized to reduce area and power consumption**
  - Core performance tuned for 5G applications



Optimizations Result in Smaller Logic Array Blocks (LABs) and Lower Power

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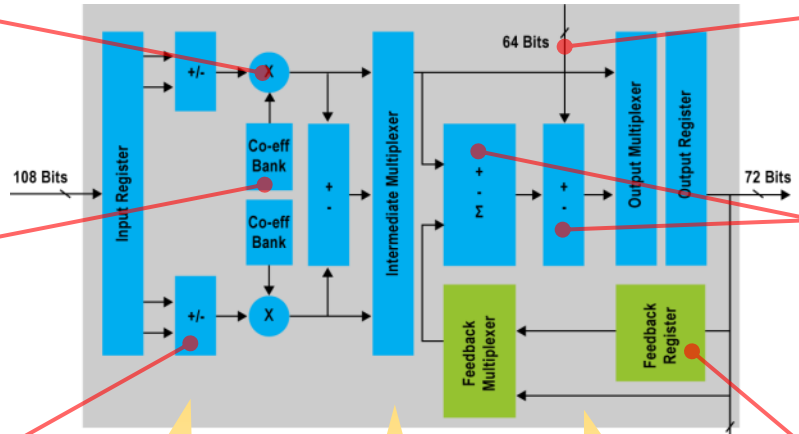
Variable-Precision DSP Block

Multiplier Modes for Flexibility
- Three 9x9 multipliers, or
- Two 18x18 multipliers, or
- One 27x27 multiplier per block

Integrated Coefficient Registers
- Save memory and routing resources
- Built-in timing closure

Hard Pre-Adders
- Reduce multiplier usage
- Save routing resources



Motion control

Wireless FIR

Video processing

64-bit Cascade Path
- Supports systolic finite impulse response (FIR)
- Sum of products

Up to 64-bit Adder / Subtractor / Accumulator
- 1,024-tap filters
- 2,048-tap symmetric filters

Feedback Register and Multiplexer
- Implement two independent filter channels per DSP block

High-Efficiency for Key Applications

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Embedded Memory

- **Two types: MLAB and M10K**

	M10K	MLAB
f_{MAX}	380 MHz	300 MHz
RAM bits per block	10,240 bits	640 bits
Configuration	256 x40 or 32 bits 512 x20 or 16 bits 1K x10 or 8 bits 2k x5 or 4 bits 4k x2 bits 8K x1 bit	32 x 1, 2, 4, 8, 9, 10, 16, 18, or 20 bits
ROM with preload	✓	✓
Single-port	✓	✓
Simple dual-port	✓	✓
True dual-port	✓	-

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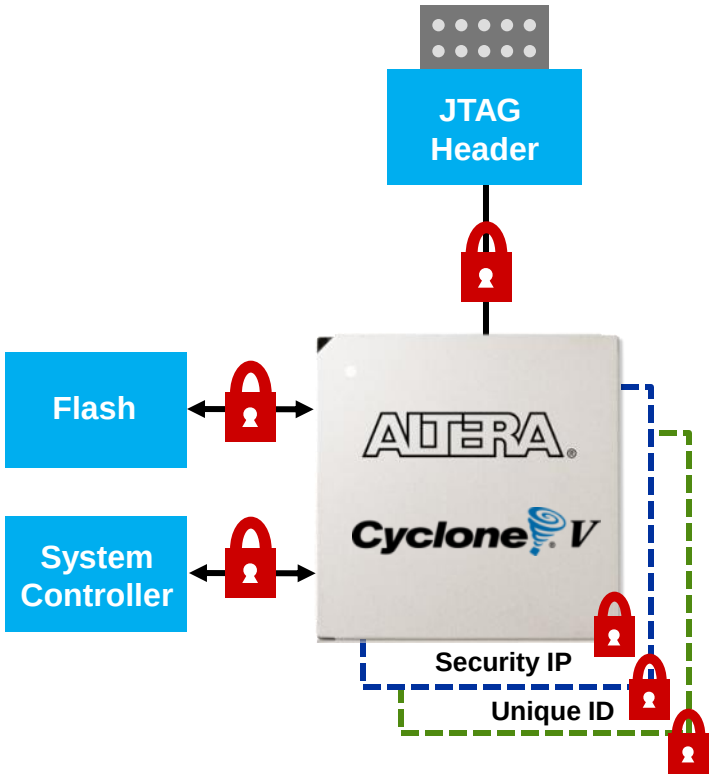
Design Security – Deny the Counterfeiters!

- **256-bit Advanced Encryption Standard (AES)**
  - Volatile and non-volatile keys
- **Embedded unique identification (ID)**
  - For traceability
- **Cyclical redundancy check (CRC)**
  - Detects unauthorized configuration changes
- **On-chip oscillator**
  - Results in uninterruptible clock source
- **Protection against tampering**
  - Clears device if tampering is detected
- **JTAG port protection**
  - Prevents reverse engineering



The Most Comprehensive Design Protection in an FPGA

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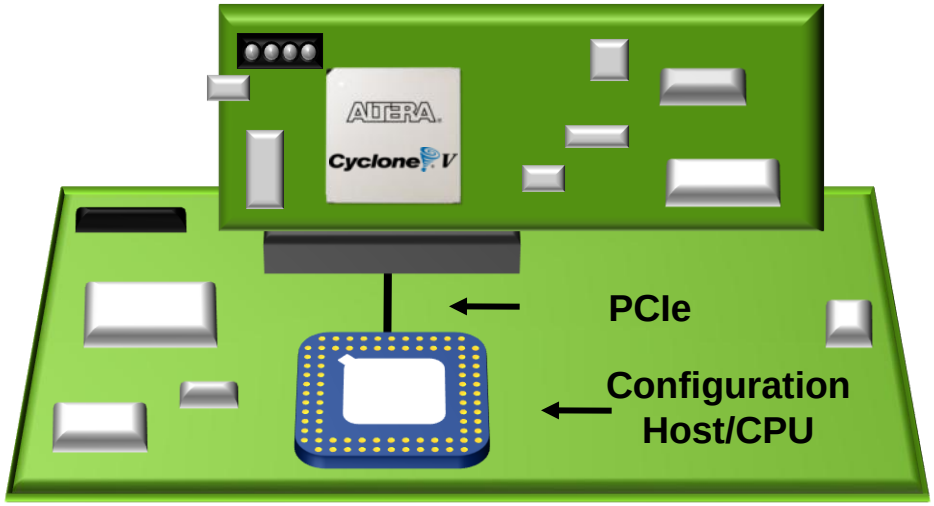
Faster, More Flexible Configuration Options

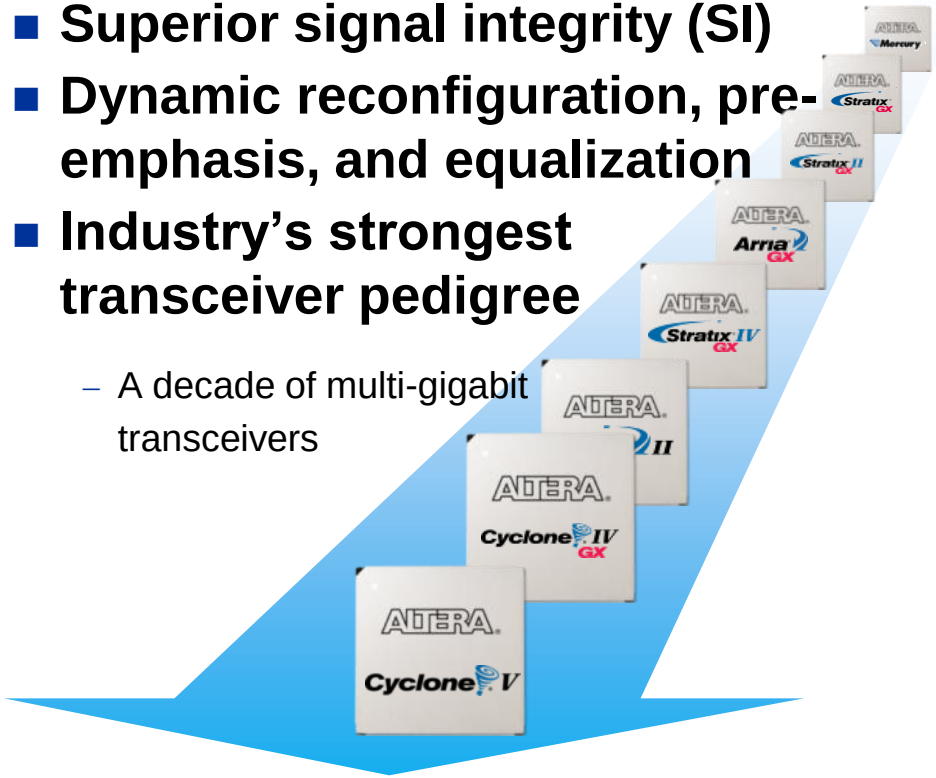
- **Configuration Via Protocol (CvP)**
  - Fast, low pin count configuration
  - Greater flexibility for configuration storage
- **Wider bus for faster configuration**
  - Active serial (AS) x1 and x4 (NEW)
  - Fast passive parallel (FPP) x8 and x16 (NEW)
- **Classic configuration options**
  - Passive serial (PS)
  - JTAG



Flexible, Low Pin Count Configurations Including PCIe Option

Cyclone V FPGA Transceivers

- 88 mW power per channel at 5G
- Superior signal integrity (SI)
- Dynamic reconfiguration, pre-emphasis, and equalization
- Industry's strongest transceiver pedigree
  - A decade of multi-gigabit transceivers



Protocol	GX Data Rate (Gbps)	GT Data Rate (Gbps)
Basic mode/ proprietary protocols	Up to 3.125	Up to 5.0
CPRI	0.6144 to 3.072	0.6144 to 6.144
OBSAI	0.75 to 3.072	
Serial RapidIO®	1.25 to 3.125	
JESD204A	0.3125 to 3.125	
PCIe	2.5	5.0
SATA	1.5 to 3.0	
SDI SD/HD, 3G-SDI (Triple Rate)	0.27 to 2.97	
XAUI	3.125	
Gigabit Ethernet	1.25	
Display Port	Up to 5.4	
Vx1	Up to 3.125	Up to 3.75

The Most Robust and Lowest Power Transceivers

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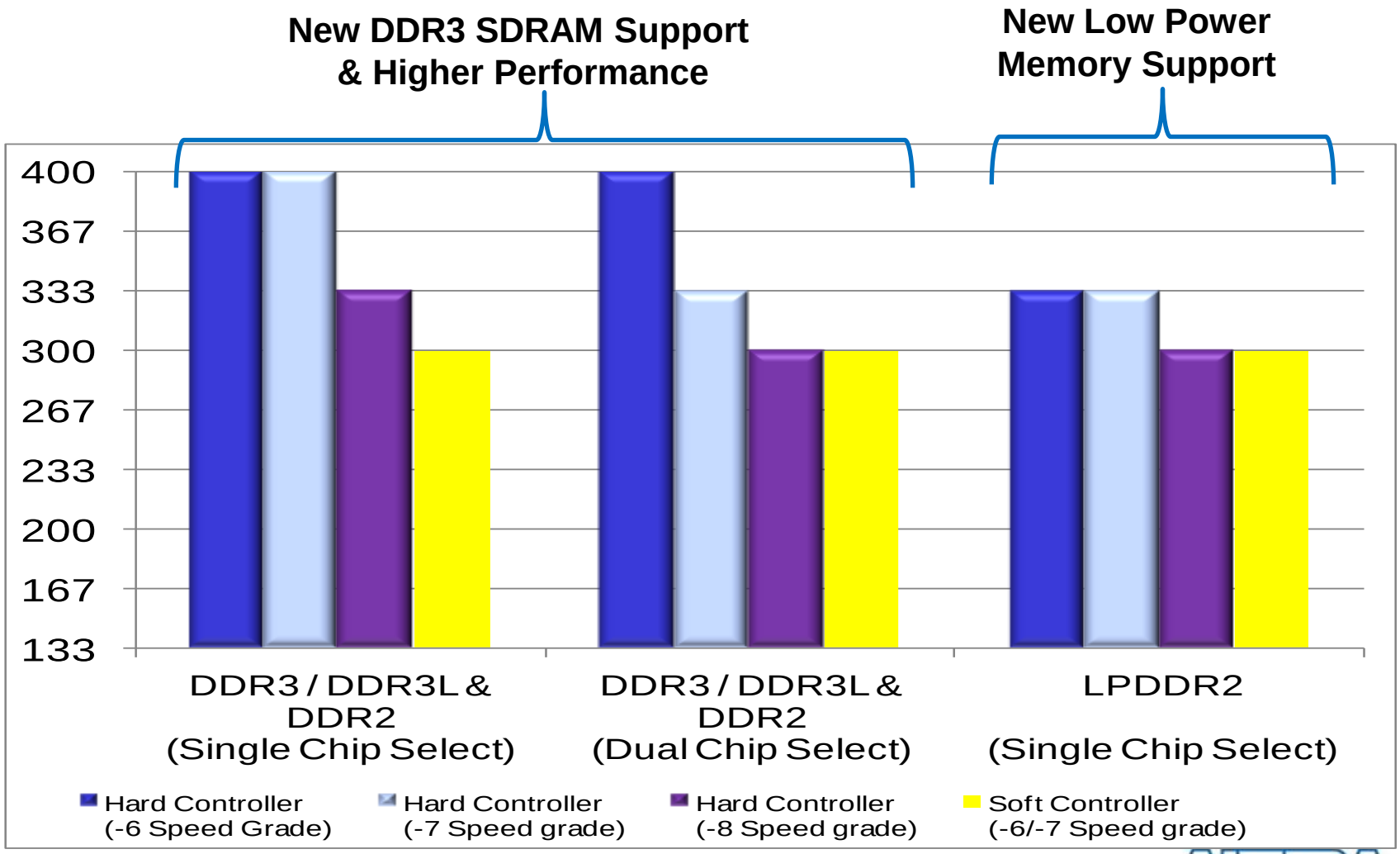
Cyclone V FPGA External SDRAM Interface



Performance & Flexibility to Meet Your Application Needs

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Cyclone V FPGAs: Ideal for Industrial Applications

Need	Cyclone V FPGA Feature	Customer Benefit
High Function and Small Form Factor	• 3.3-V I/O with 16mA drive • PCIe multifunction • Integrated security and safety • HiSPi™, Sub-LVDS I/O • Just two voltages for core and transceiver power	• Less components → reduced BOM cost • Single hardware supports multiple SKU's
Low Power	• Up to 40% lower total power	• Easier thermal management • Increased functionality while staying within fixed power budgets
Long Life	• >15 years of life cycle • Integrated security and safety	• Obsolescence proof • Supports legacy ASSP I/Os • Prevents cloning and reverse engineering

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Cyclone V FPGA Device Family Plan

Family	Device	Core Fabric						Interconnect			Hard IP	
		LE (1)	# Blocks	Block Memory (Kb)	MLAB (Kb)	DSP Blocks (2)	PLL	XCVR	GPIO	LVDS Pairs	PCIe Blocks (Base / Full)	Memory Controllers (Base / Full) (4)
Cyclone V E	5CEA2	25K	176	1,760	196	25	4	-	224	100	-	0,1
	5CEA4	49K	308	3,080	303	66	4	-	224	100	-	0,1
	5CEA5	77K	446	4,460	424	150	6	-	240	100	-	0,2
	5CEA7	149.5K	686	6,860	836	156	7	-	480	122	-	0,2
	5CEA9	301K	1,220	12,200	1,717	342	8	-	480	122	-	0,2
Cyclone V GX	5CGXC3	31.5K	119	1,190	159	51	4	3	208	48	0,1	0,1
	5CGXC4	50K	250	2,500	295	70	6	6	336	90	0,2	0,2
	5CGXC5	77K	446	4,460	424	150	6	6	336	100	0,2	0,2
	5CGXC7	149.5K	686	6,860	836	156	7	9	480	122	0,2	0,2
	5CGXC9	301K	1,220	12,200	1,717	342	8	12	560	122	0,2	0,2
Cyclone V GT	5CGTD5	77K	446	4,460	424	150	6	6	336	100	2	2
	5CGTD7	149.5K	686	6,860	836	156	7	9	480	122	2	2
	5CGTD9	301K	1,220	12,200	1,717	342	8	12	560	122	2	2

1. 2.65 logic element (LE) equivalent per Adaptive Logic Module (ALM).
2. Each DSP block can natively support 3x(9X9), 2x(18x18), or single 27 x 27 multiplier.
3. Hard Memory Controllers include ECC support for high reliability.
4. Number of Hard Memory Controllers available in the device (0,1, or 2) can be chosen in part ordering code

Preliminary

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Cyclone V FPGA Package Options

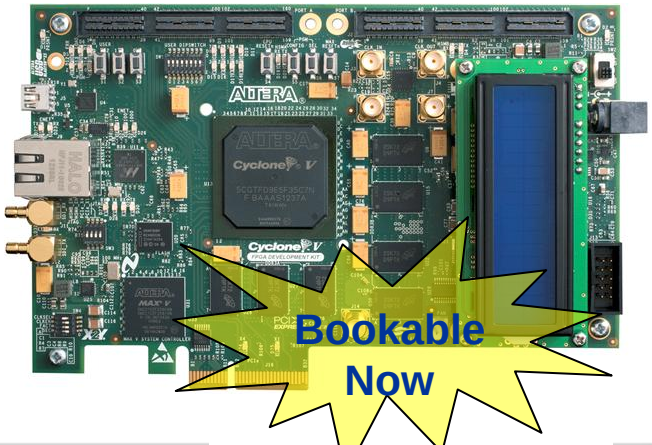
Family	Device	LE	M301 11x11	M383 13x13	M484 15x15	F256 17x17	U324 15x15	U484 19x19	F484 23x23	F672 27x27	F896 31x31	F1152 35x35
Cyclone V E	5CEA2	25K	-	223 [3]	-	128	176	224	224	-	-	-
	5CEA4	49K	-	223 [3]	-	128	176	224	224	-	-	-
	5CEA5	77K	-	175	-	-	-	224	240	-	-	-
	5CEA7	149.5K	-	-	240	-	-	240	240	336	480	-
	5CEA9	301K	-	-	-	-	-	240	224	336	480	-
Cyclone V GX	5CGXC3	31.5K	-	-	-	-	144 / 3	208 / 3	208 / 3	-	-	-
	5CGXC4	50K	129 / 4	175 / 6	-	-	-	224 / 6	240 / 6	336 / 6	-	-
	5CGXC5	77K	129 / 4	175 / 6	-	-	-	224 / 6	240 / 6	336 / 6	-	-
	5CGXC7	149.5K	-	-	240 / 3	-	-	240 / 6	240 / 6	336 / 9	480 / 9	-
	5CGXC9	301K	-	-	-	-	-	240 / 5	224 / 6	336 / 9	480 / 12	560 / 12
Cyclone V GT	5CGTD5	77K	129 / 4	175 / 6	-	-	-	224 / 6	240 / 6	336 / 6	-	-
	5CGTD7	149.5K	-	-	240 / 3	-	-	240 / 6	240 / 6	336 / 9	480 / 9	-
	5CGTD9	301K	-	-	-	-	-	240 / 5	224 / 6	336 / 9	480 / 12	560 / 12

Notes:

1. *New Packages*
2. *See Quartus II design software for pin-migration details.*
3. *175 I/O are migratable to 5CE-A5 M383.*
4. *Fxxx = 1.0mm ball spacing*
5. *Uxxx = 0.8mm ball spacing*
6. *Mxxx = 0.5mm ball spacing*

Cyclone V Dev Kit Portfolio is Strong!

	Cyclone V E Kit	Cyclone V GX Kit	Cyclone V GT Kit
DDR3 SDRAM	Soft memory controller: x32	Hard Mem. Controller: x32 w/t ECC @ 400 MHz Soft Mem. Controller: x32 w/t ECC	Hard Mem. Controller: x32 w/t ECC @ 400 MHz Soft Mem. Controller: x64 (no ECC)
LPDDR2 SDRAM	LPDDR2 x16 (soft memory controller)	-	-
User Control	4 push buttons, 5 LEDs, 4 DIP switches, 2x Resets (CPU reset, System reset)	3 push buttons, 4 LEDs, 4 DIP switches, 2x Resets (CPU reset, Dev Clear)	3 push buttons, 4 LEDs, 4 DIP switches, 2x Resets (CPU reset, Dev Clear)
LCD	Character LCD (16x2)	Character LCD (16x2)	Character LCD (16x2)
Components and interfaces	Ethernet (2x RJ45), HSMC (1), UART USB 2.0 for configuration and control	PCIe x4 Edge Connector, HSMC (1), Ethernet (RJ45), SDI (1), SMA (2 for 1 Tx/Rx) USB 2.0 for config. & control	PCIe x4 Edge Connector, HSMC (2), Ethernet (RJ45), SDI (2), SMA (2 for 1 Tx/Rx), USB 2.0 for config. & control
Public Availability	Shipping since Nov. 2012	Shipping since Sept. 2012	**April 2013**
Price, P/N	**$1,099** (DK-DEV-5CEA7N)	**$1,199** (DK-DEV-5CGXC7NES)	**$1,299** (DK-DEV-5CGTD9N)



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MAX V CPLDs

Announcing the MAX V CPLD Family

Low power and high performance

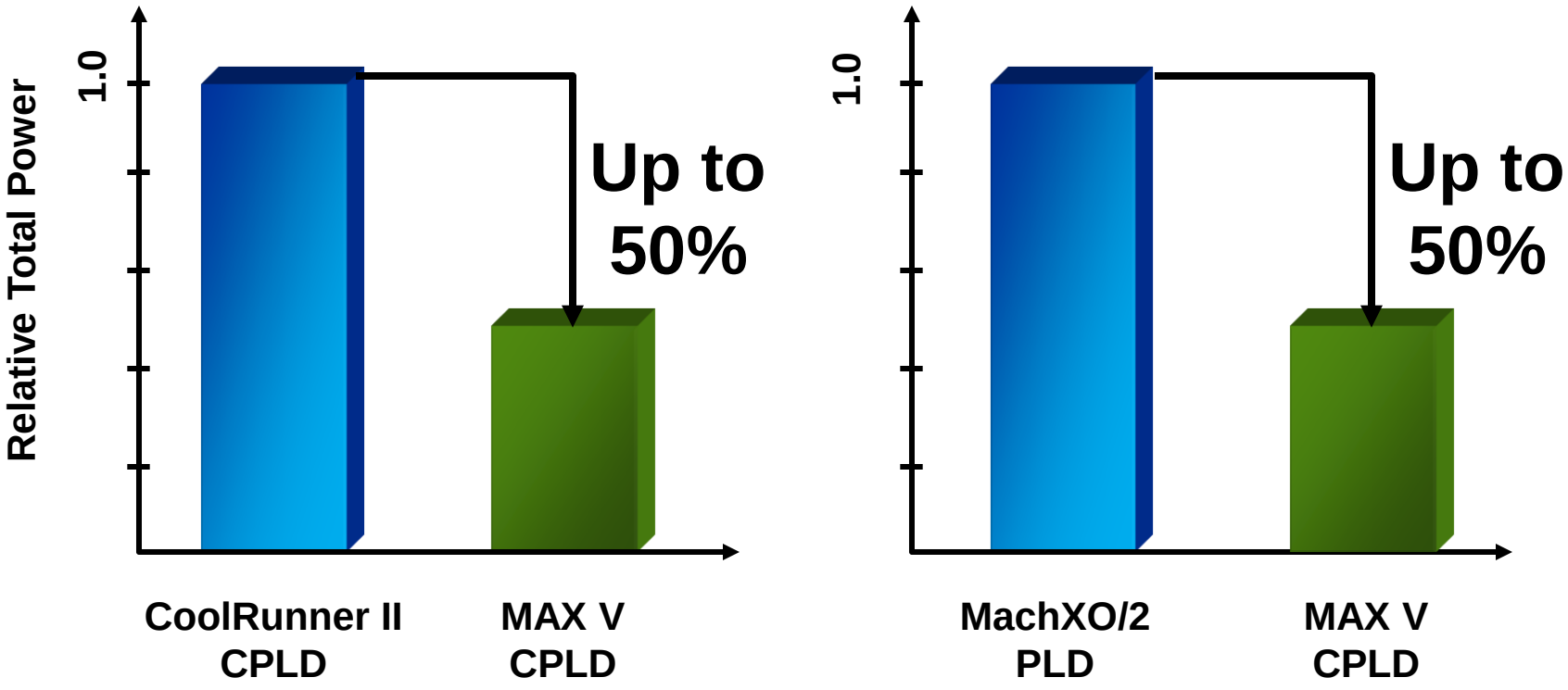
Up to 50% lower total power *

Performance up to 247.5 MHz

*** Versus competitors' equivalent density CPLDs**

ALTERA®
MEASURABLE ADVANTAGE™

Low-Power Leadership



*** Based on suppliers early power estimators at 85° C, 100MHz**

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MAX V Family – Package and I/O Options

Device	Density		M64 4.5x4.5	E64 7x7	M68 5x5	T100 14x14	M100 6x6	T144 21x21	F256 17x17	F324 19x19
	Logic Elements	Typical Macrocells								
5M40Z	40	32	30	54						
5M80Z	80	64	30	54	52	79				
5M160Z	160	128		54	52	79	79			
5M240Z	240	192			52	79	79	114		
5M570Z	570	440				74	74	114	159	
5M1270Z	1,270	980						114	211	271
5M2210Z	2,210	1,700							203	271

M = 0.5-mm pitch easy-break-out BGA package
E = 0.5-mm pitch EQFP package
T = 0.5-mm pitch TQFP package
F = 1.0-mm pitch FineLine BGA package

Supports Commercial, Industrial, and Extended Temperatures (T_j = -40° C to +125° C)

ALTERA
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Consumer functions: Simple → Complex

I/O Expansion

Processor — 3 → **CPLD** *or FPGA* → 10's – 100's I/Os

Bridging

ASIC — I^2C → **CPLD** *or FPGA* — SPI → ASSP

Motor control

Processor ↔ **FPGA** *or CPLD* — PWM

Image co-processor

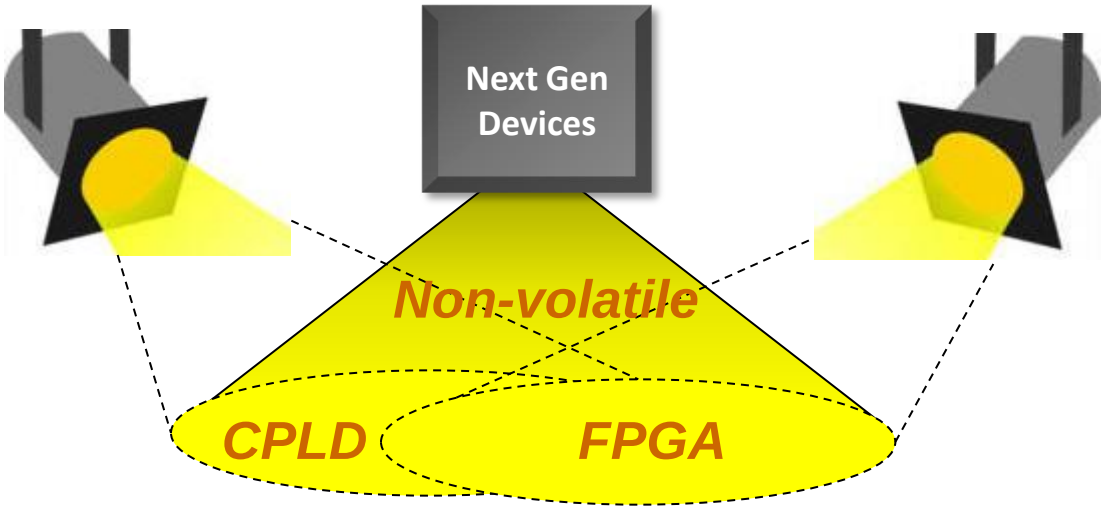
Processor ↔ **FPGA** *or CPLD* — Display I/F

Video overlays, enhancements,

Chassis Management

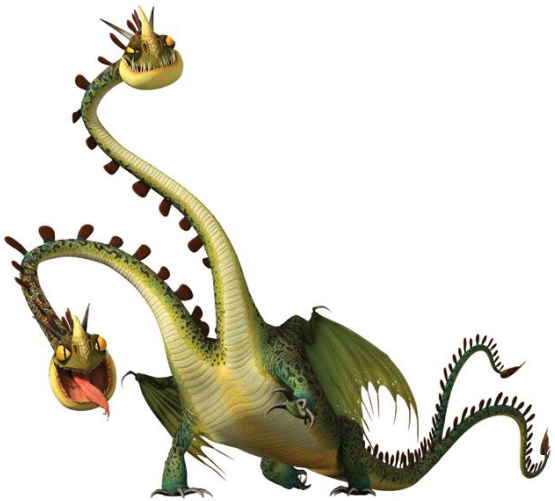
Next Generation CPLDs

Next Generation Low-Cost PLD Family



TSMC 55nm EmbFlash Technology

COMING SOON!!!



ALTERA
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Thank You