Digital IF Modem Applications

Agenda

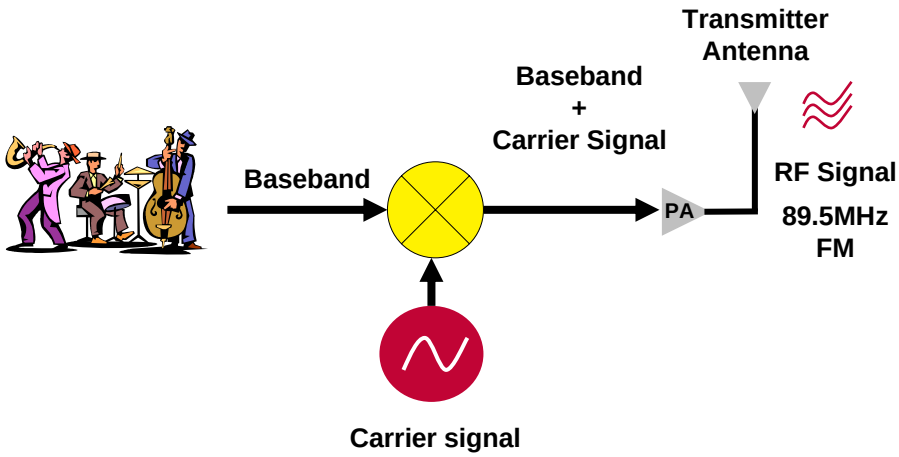
- Digital IF modem applications overview
- FPGA as a digital IF modem solution
- Live demo
- Conclusions

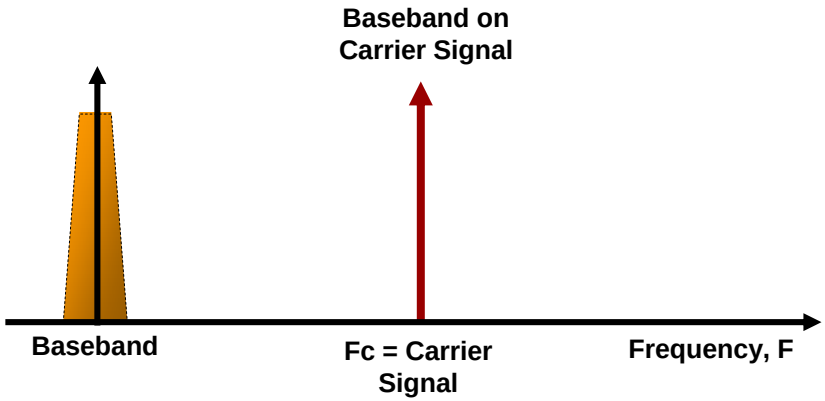
Digital IF Modem Applications Overview

Digital IF Modem Defined

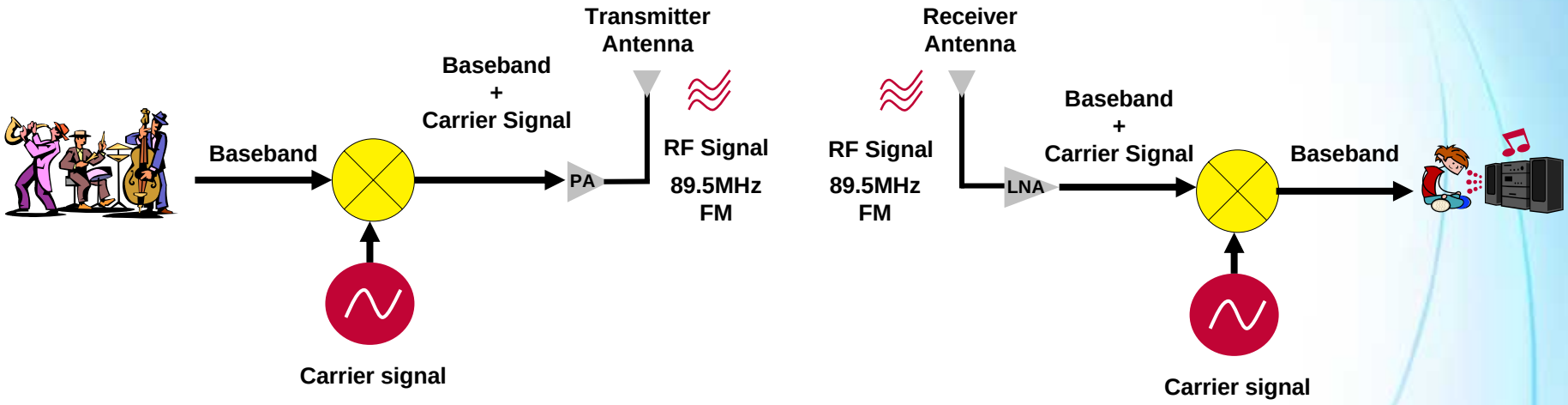
- **IF**: [from Wikipedia] An intermediate frequency (IF) is a frequency to which a carrier frequency is shifted as an intermediate step in transmission or reception
- **Digital IF modem**: A device that processes IF signals in their digital representations with digital methods

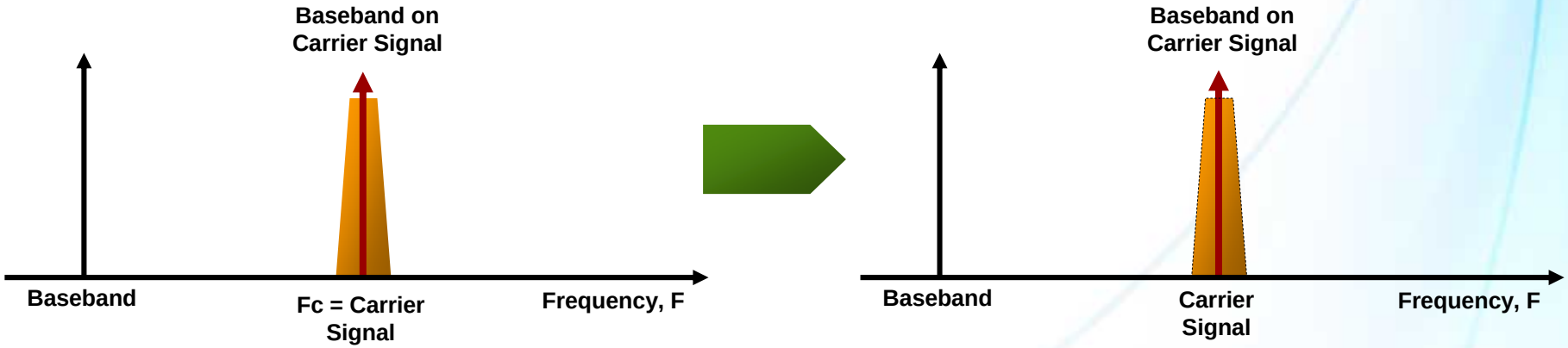
Background





Background





Digital IF Market Applications

Cellular communication

- Global System for Mobile Communications (GSM)
- W-CDMA
- Code Division Multiple Access-2000 (CDMA-2000)
- EVD
- Long-term evolution (LTE)

Video broadcast

- Digital video broadcast (DVB) – H/T/S modulators and demodulators

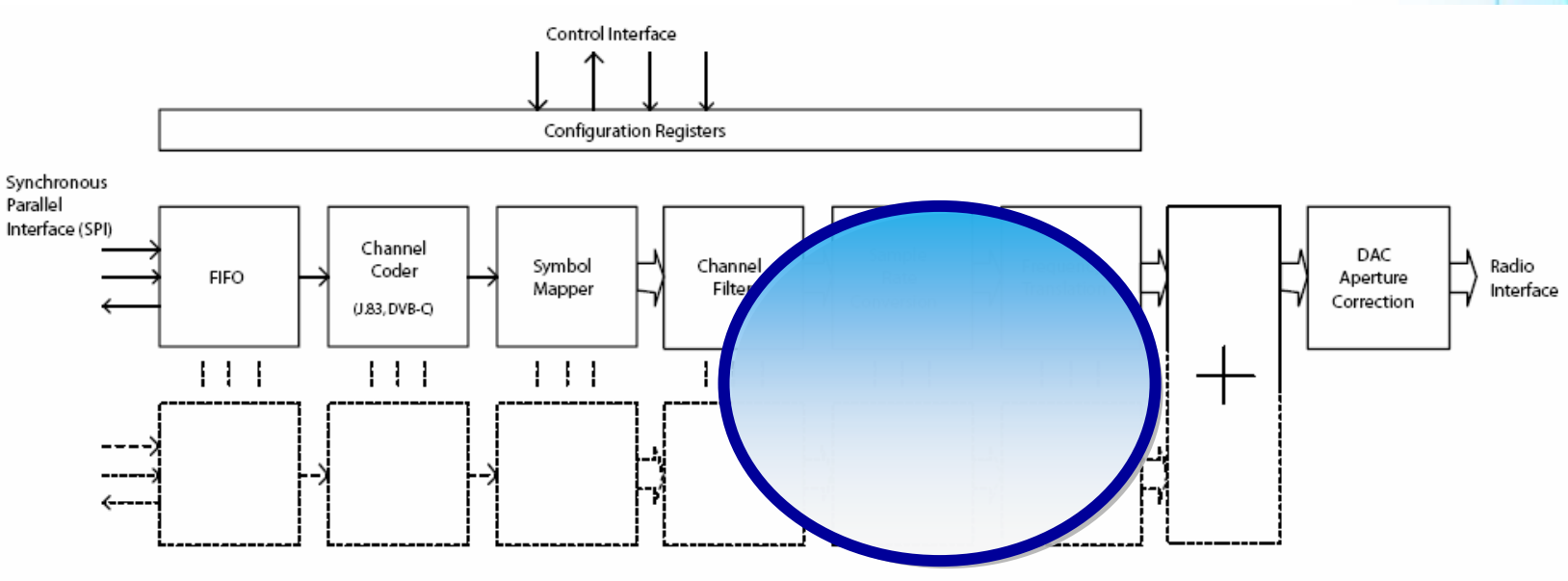
Military secure communication

- Field sensors
- Hand-held/portable radios
- Military global positioning system (GPS)
- Military radios
- Satellite
- Radar/sonar

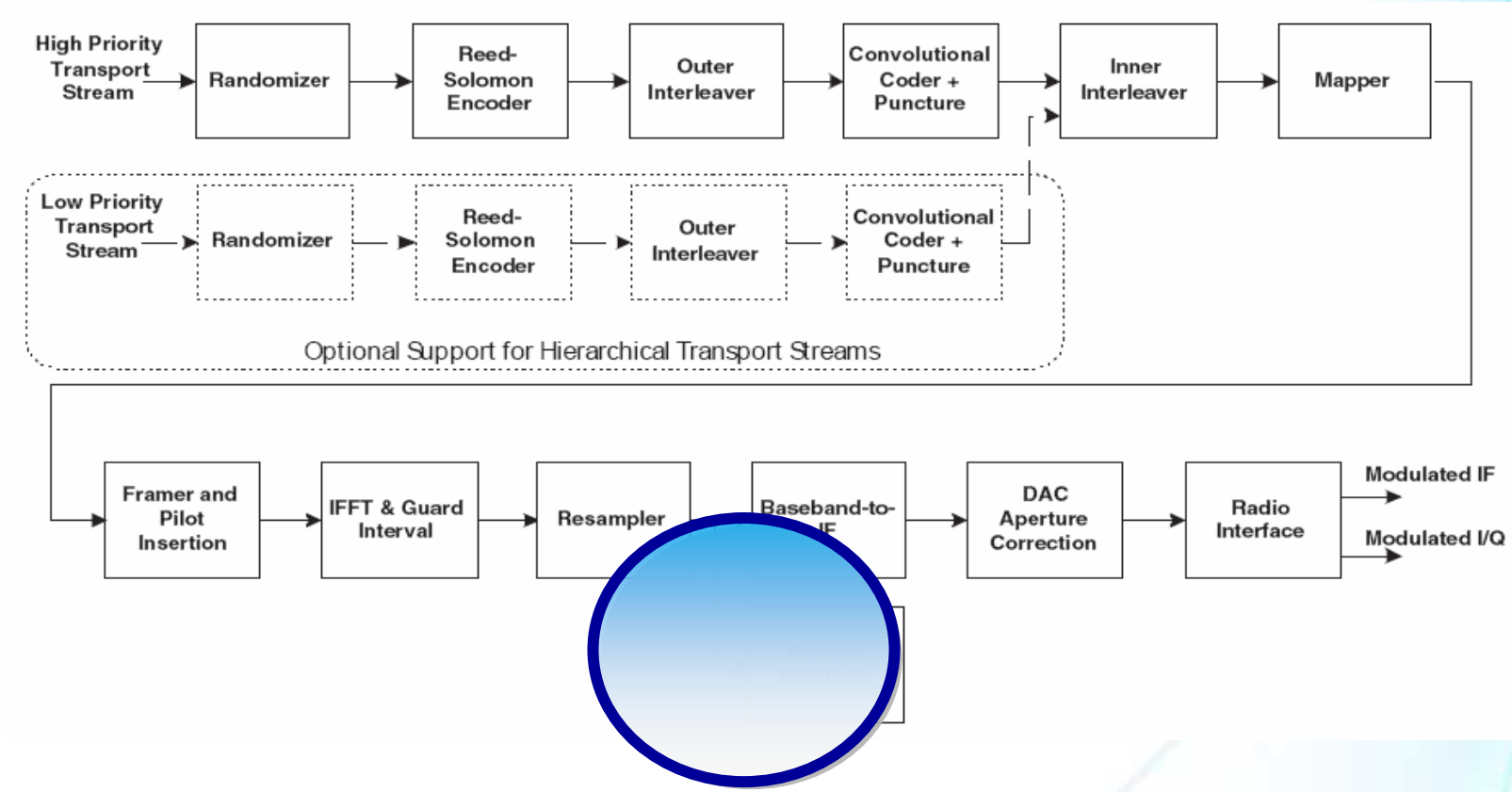
Medical instrument

- Computed tomography (CT) scan
- Ultrasound
- Magnetic resonance imaging (MRI)
- Medical wireless instruments

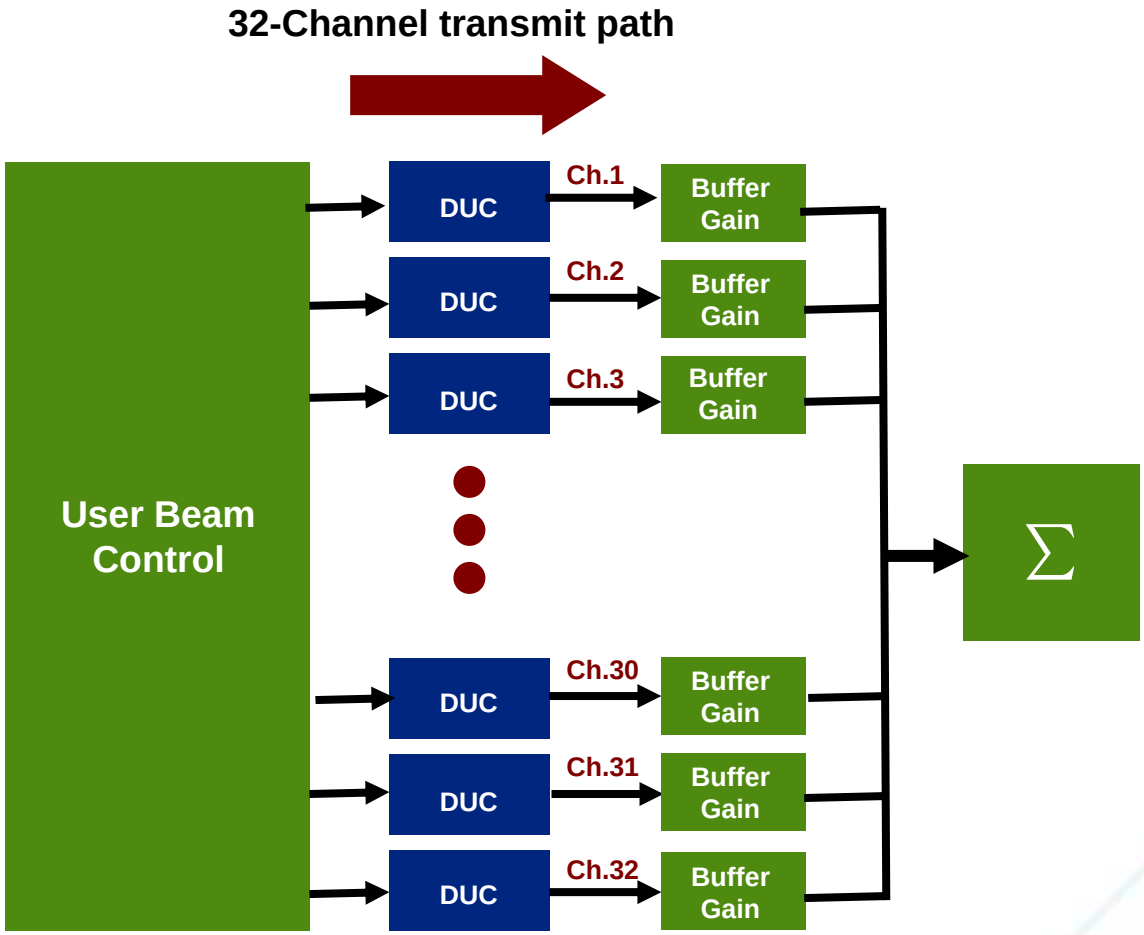
Application Example #1: Cable Modulator

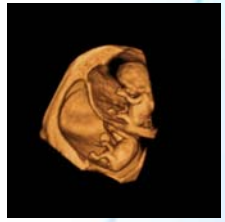


Application Example #2: DVB-T/H/S



Application Example #3: Medical Ultrasound

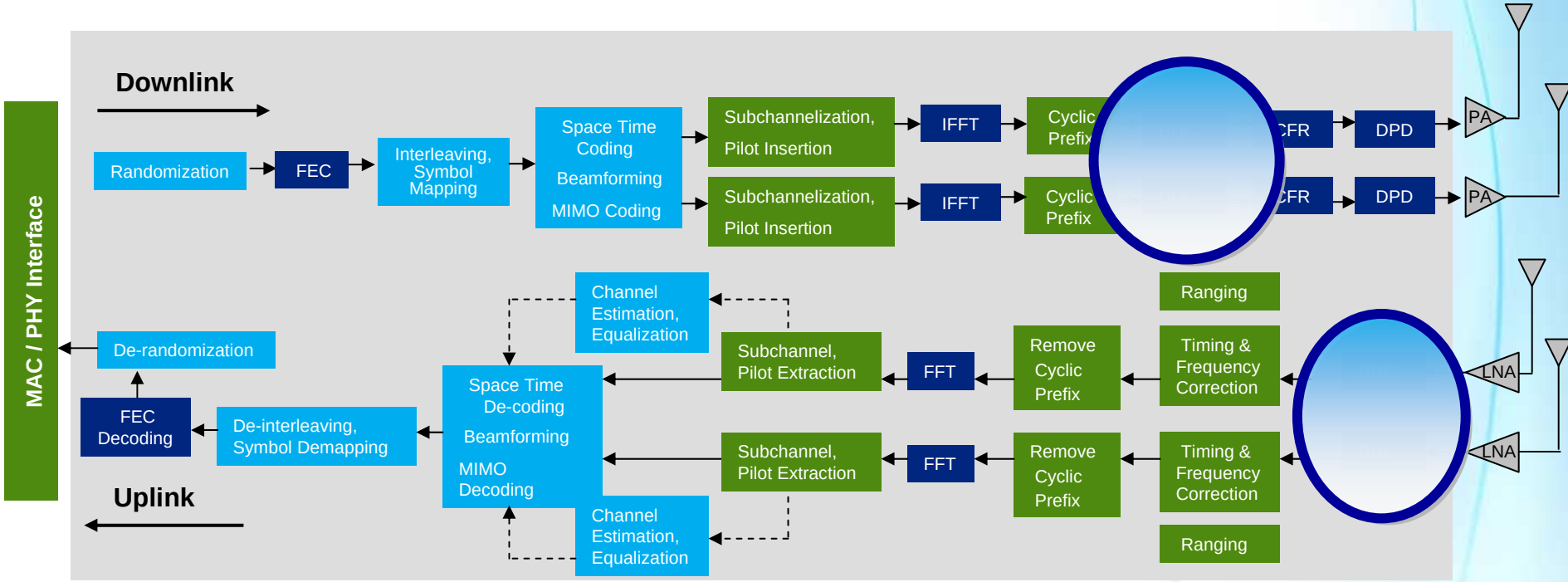




Ultrasound transducer

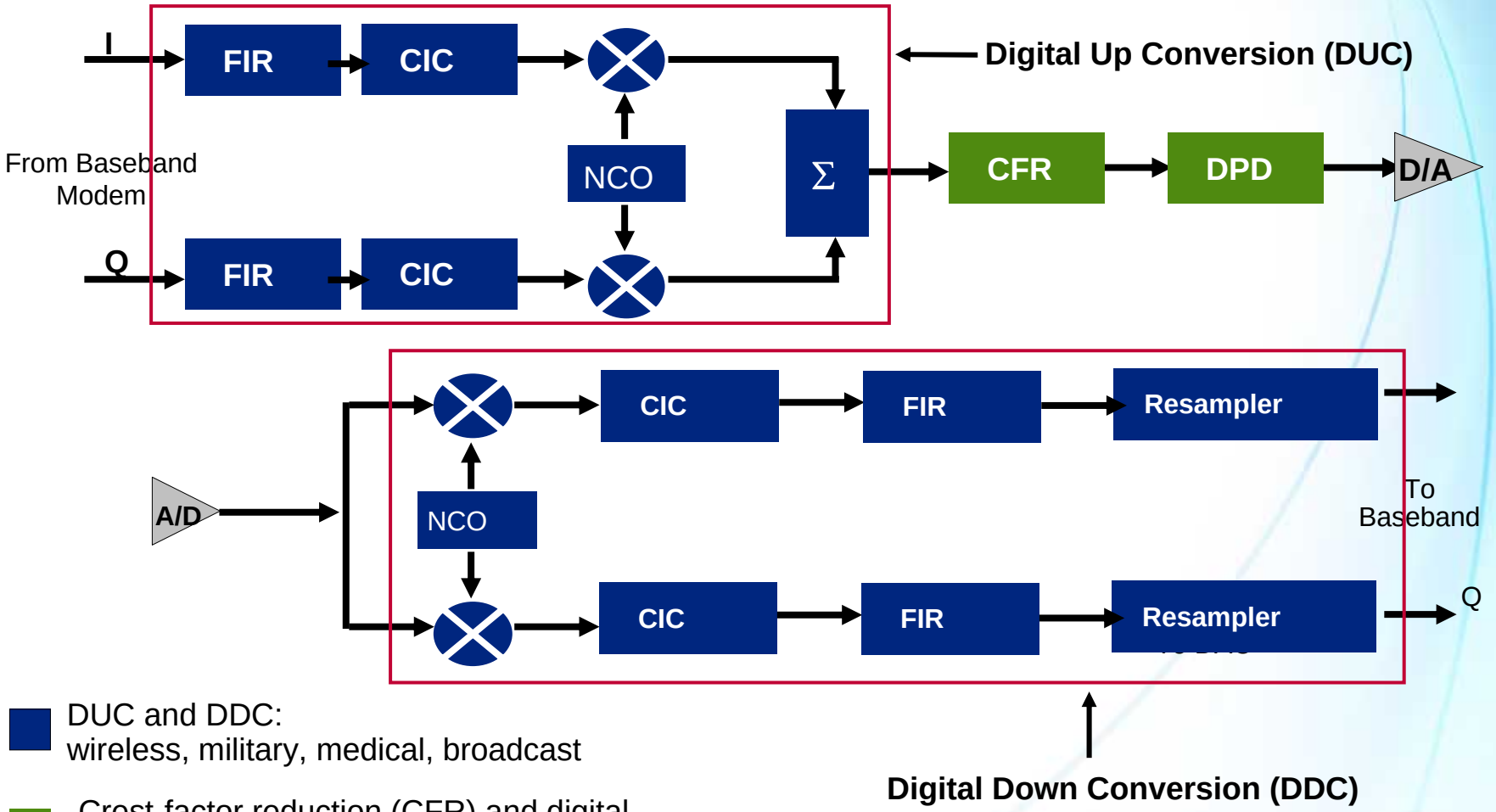
Comprehensive Altera solution

Application Example #4: WiMAX Orthogonal Frequency Division Multiplexing (OFDM) Engine

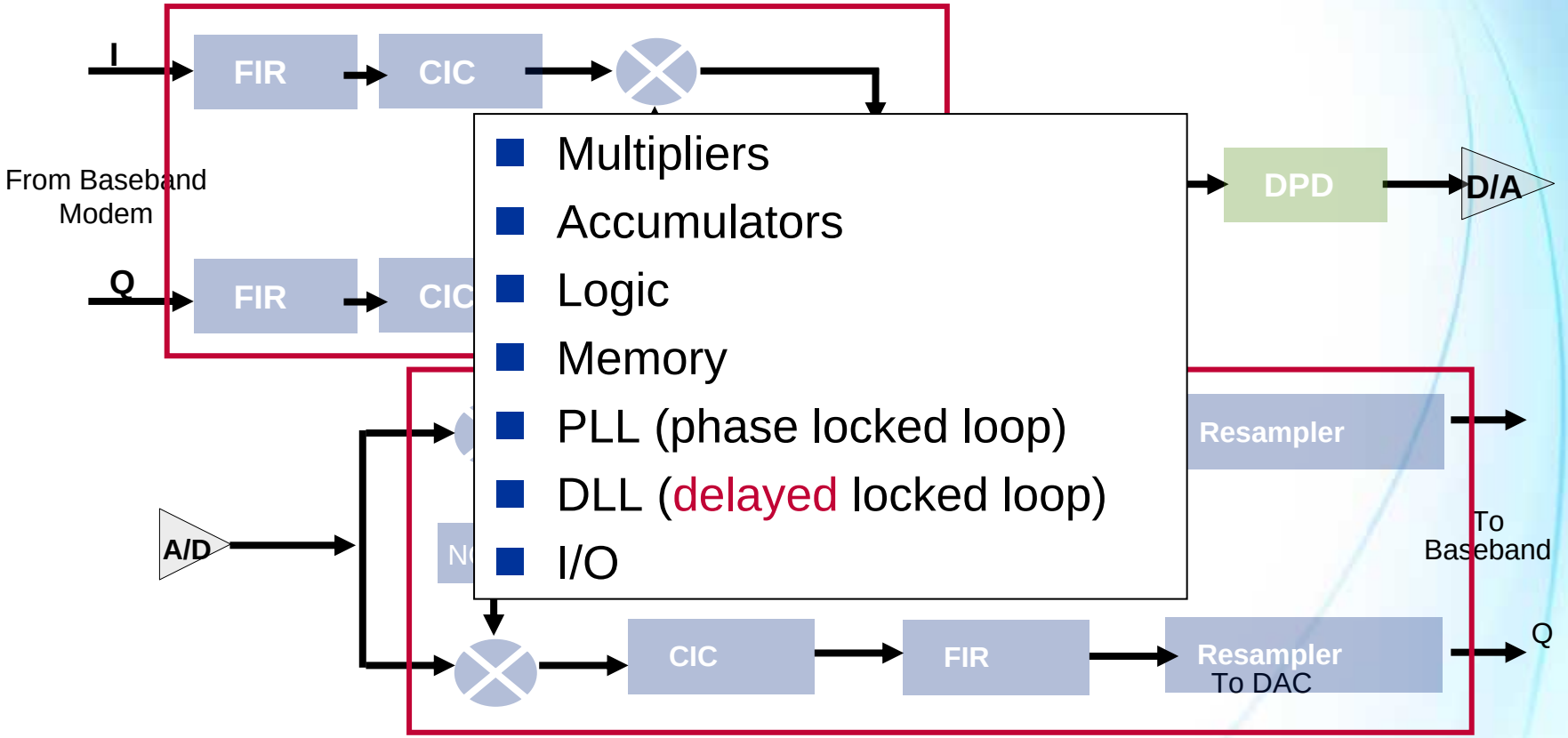


FPGA as a Digital IF Modem Solution

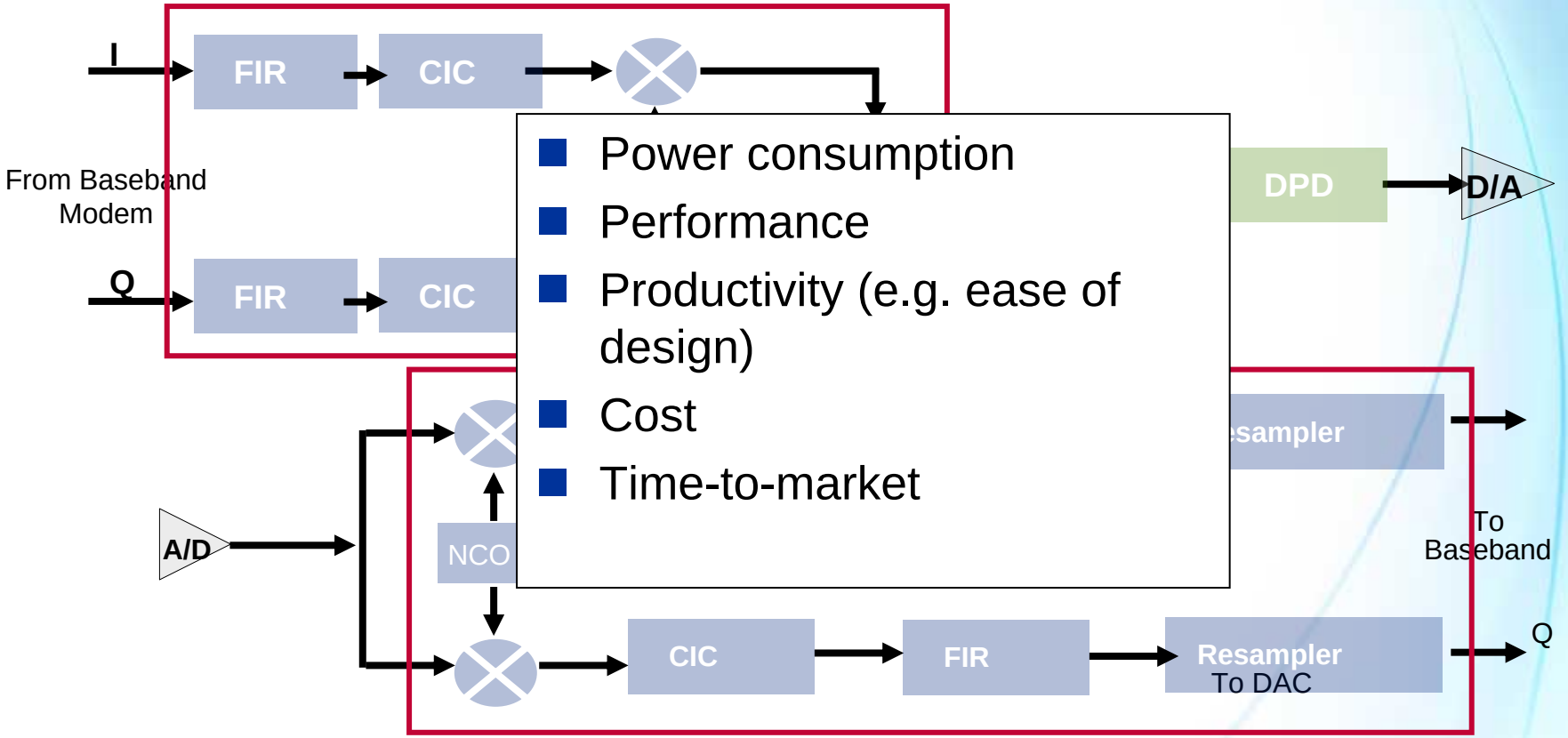
High-Level Block Diagrams of a Typical Digital IF Modem



To Build These With an FPGA, We Need…



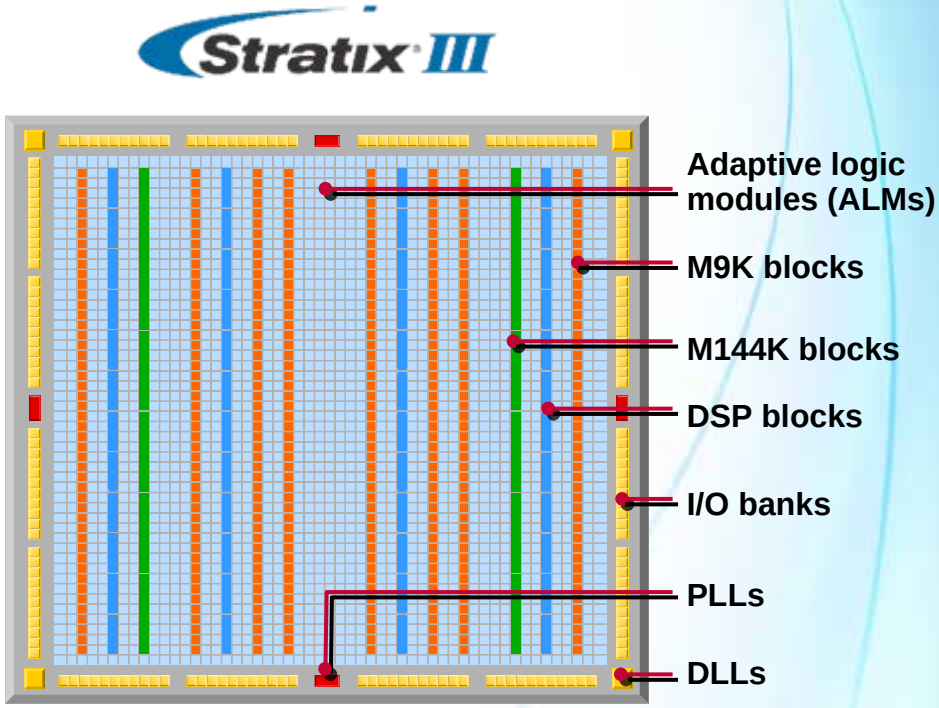
Other Considerations…



- Power consumption
- Performance
- Productivity (e.g. ease of design)
- Cost
- Time-to-market

FPGA is Ideal for Digital IF Functions Because…

- Abundance of resources for building IF functions
  - Logic: up to 338K logic elements (LEs) and 270K registers
  - Digital signal processing (DSP): up to 896 18X18 multipliers
  - Memory: up to 17.2 Mbits of 600-MHz memory
  - PLLs, DLLs: numerous located across the device for ease of clock management
  - I/O: support for wide varieties of single-ended and differential I/O standards
- Latest manufacturing process (e.g. 65 nm) + state-of-the-art design software tools for
  - Low power
  - Low cost
  - Ease of design

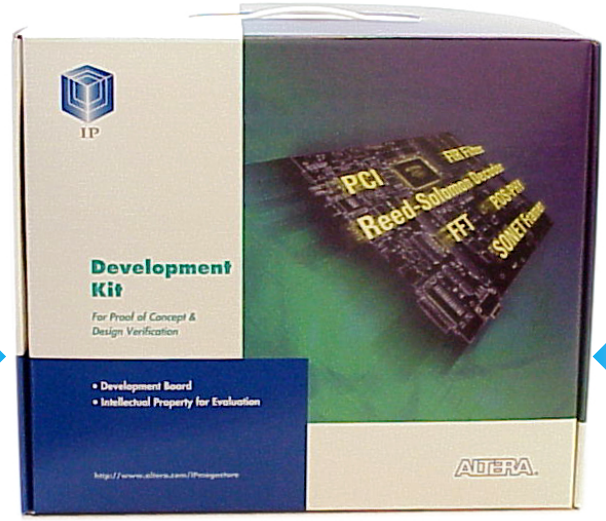


Example: WiMAX PHY Layer Implementation

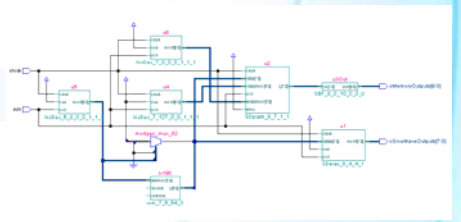
		LEs	Number of M9K memory blocks	18x18 multipliers	Power (watts)
IF processing	WiMAX DUC	2,704	50	30	0.40
	WiMAX DDC	2,623	46	25	0.40
OFDMA symbol-rate processing	DL OFDMA engine	4,176	33	4	0.25
	UL OFDMA engine	3,834	57	4	0.25
	Channel estimation and equalization	7,400	1	4	0.33
Bit-rate processing	Symbol mapper and demapper	1,404	3	0	0.10
	Forward error correction (FEC, encoding and decoding)	18,511	26	0	0.60
	Total percentage of Cyclone® III EP3C55 resources	77%	83%	43%	2.33

Altera DSP Development Kits

Contains Everything You Need to Develop High-Performance DSP Designs on FPGAs



30-Day evaluation version



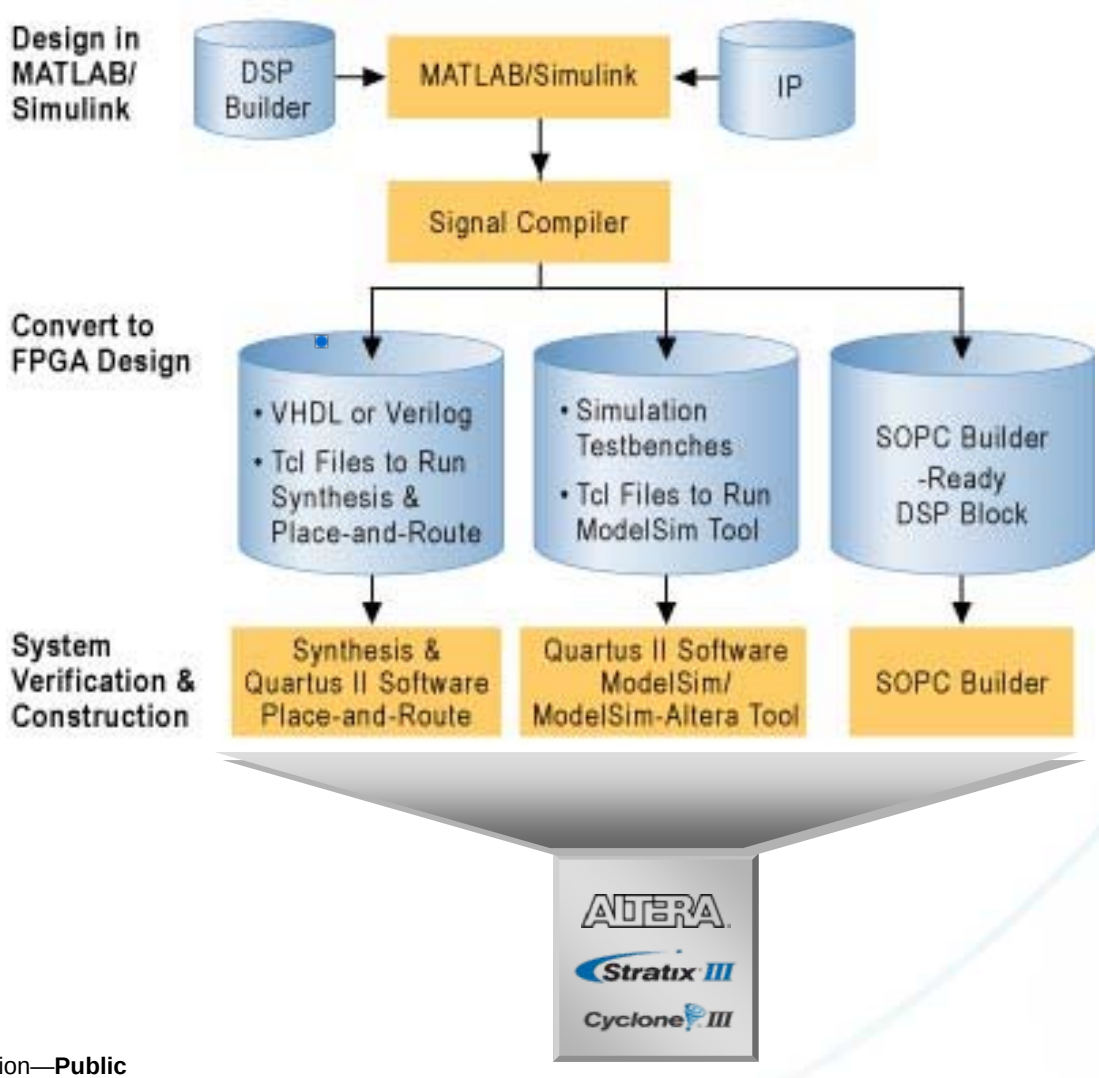
System reference designs

QUARTUS® II

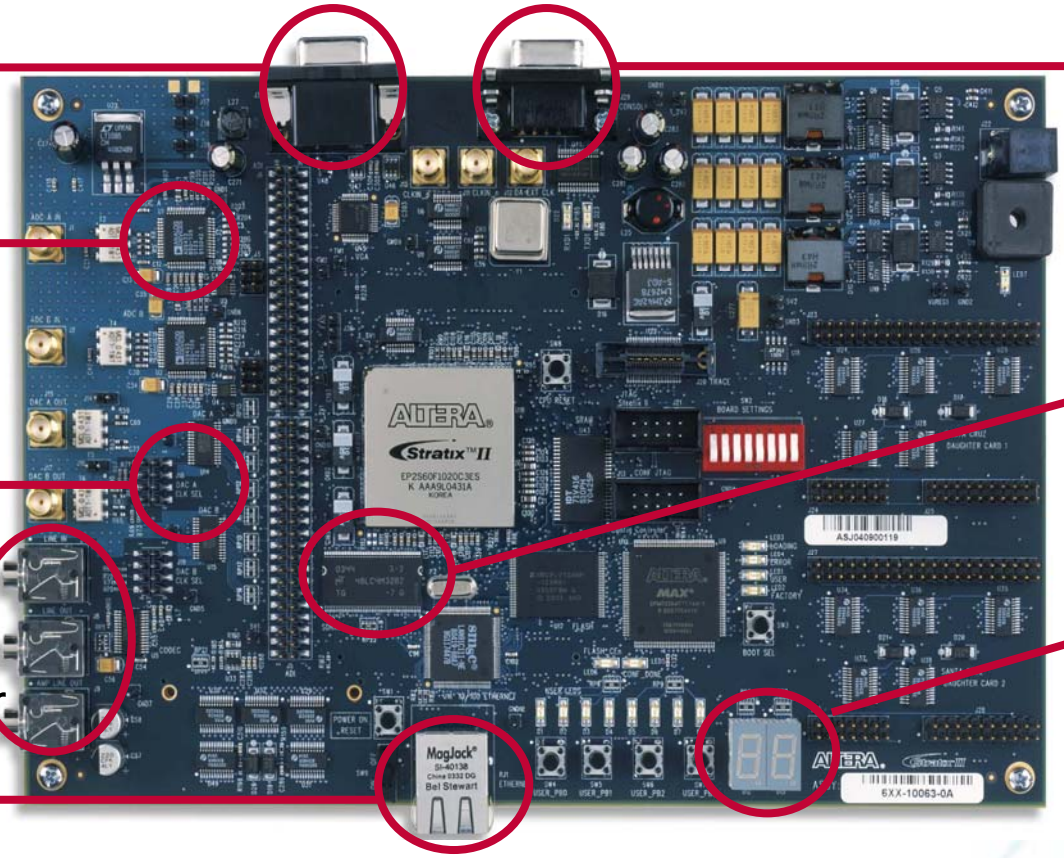
OpenCore® plus

ALTERA®

DSP Builder and Simulink Design Flow



Stratix II DSP Development Board



Cyclone III Edition Available Soon

Live Demo

Conclusion

- FPGAs deliver low power, high performance, and cost-efficient digital IF functions to enable customers' innovation
- Innovative DSP design tool flow improves productivity
- DUC and DDC application demo example
  - Design methodology significantly reduces the development time for different standards
  - Highly optimized and cost-efficient designs

Visit Altera's DSP Solution Center at

http://www.altera.com/dsp

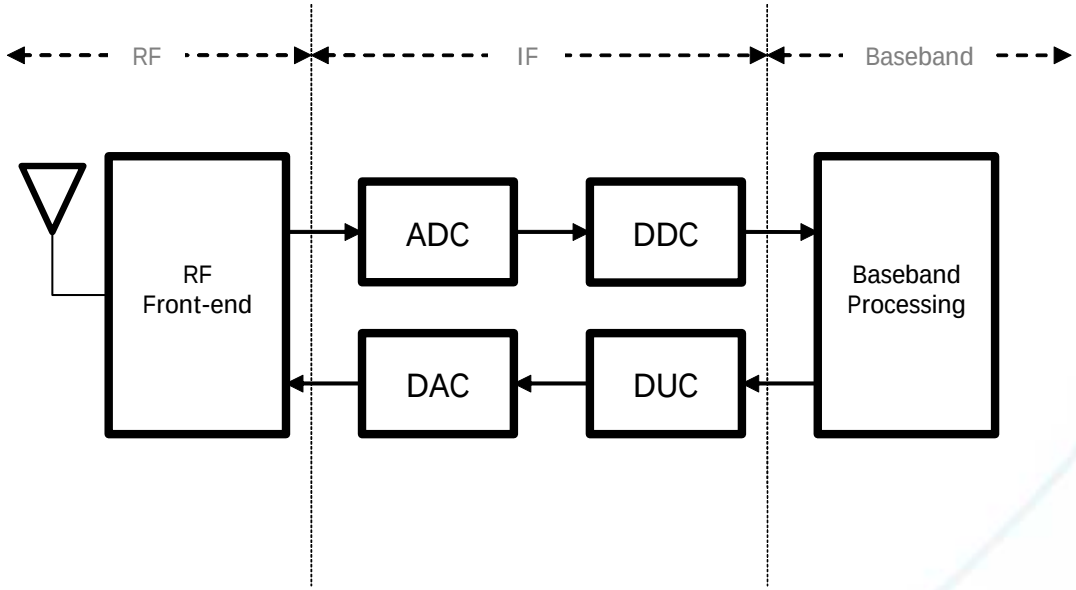
Backup slides for the Live Demo

Live Demo

- DDC/DUC reference design
- DSP Builder

Reference Design Overview

- DUC/DDC
  - Provides the link between digital baseband and analog RF front end of generic transceiver
  - High-throughput signal processing required makes FPGA ideal platform



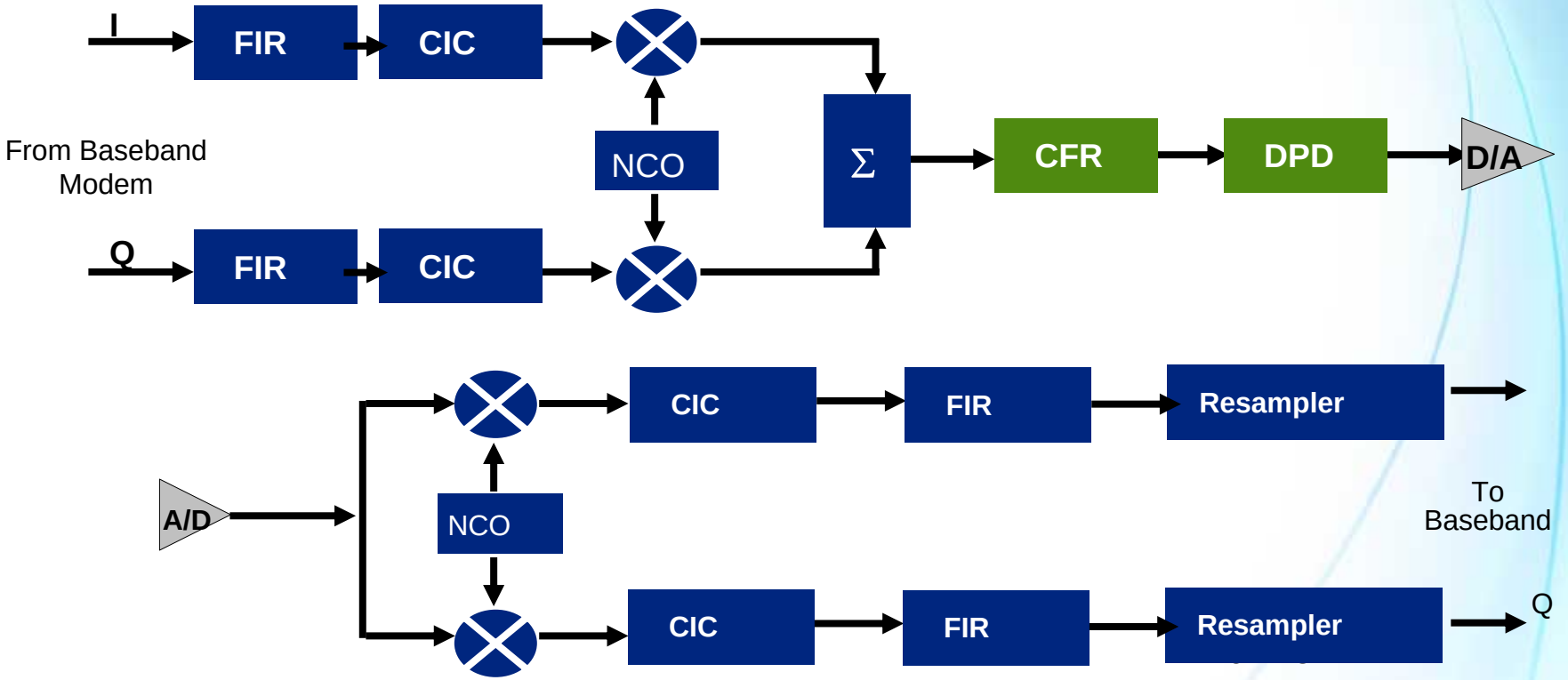
WiMAX DUC and DDC Designs

DSP Builder Ready

- Compliant to the draft WiMAX standard (IEEE 802.16)
- Multi-channel filter design for low cost
- Support for multiple transmit and receive antenna configurations
- Easily modifiable to support scalable channel bandwidths
- Uses DSP Builder methodology
- Backed up by DSP Builder-ready, highly parameterizable intellectual property (IP) MegaCore® functions

ALTERA

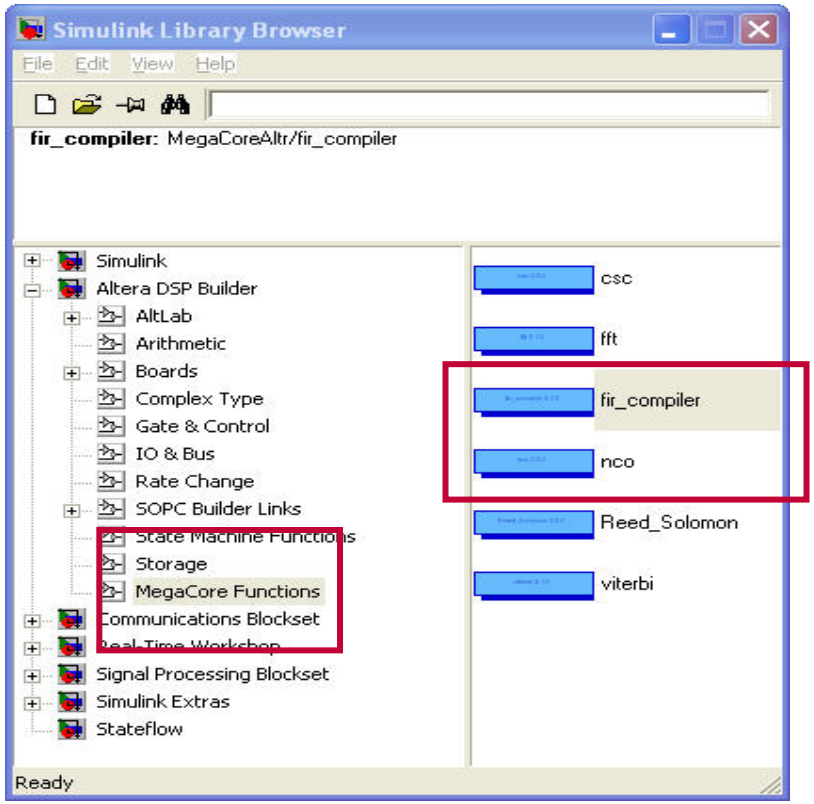
DUC and DDC High-Level Block Diagrams

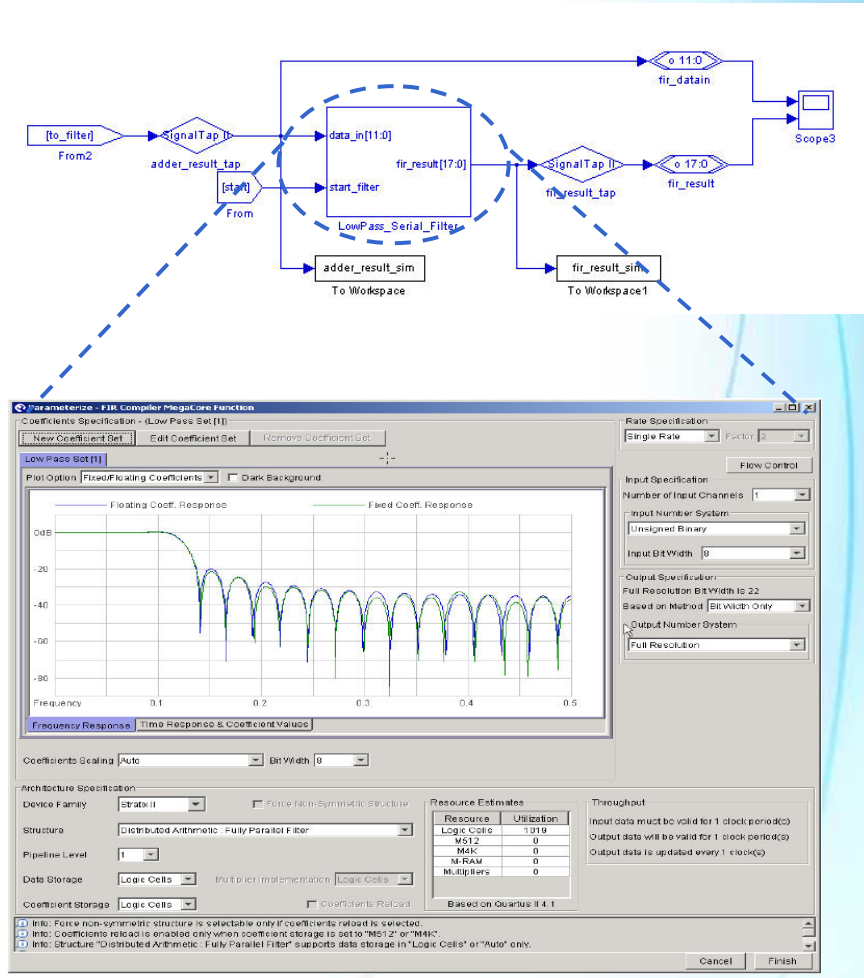


DUC and DDC:
wireless, military, medical, broadcast

Crest-factor reduction (CFR) and digital predistortion (DPD): wireless

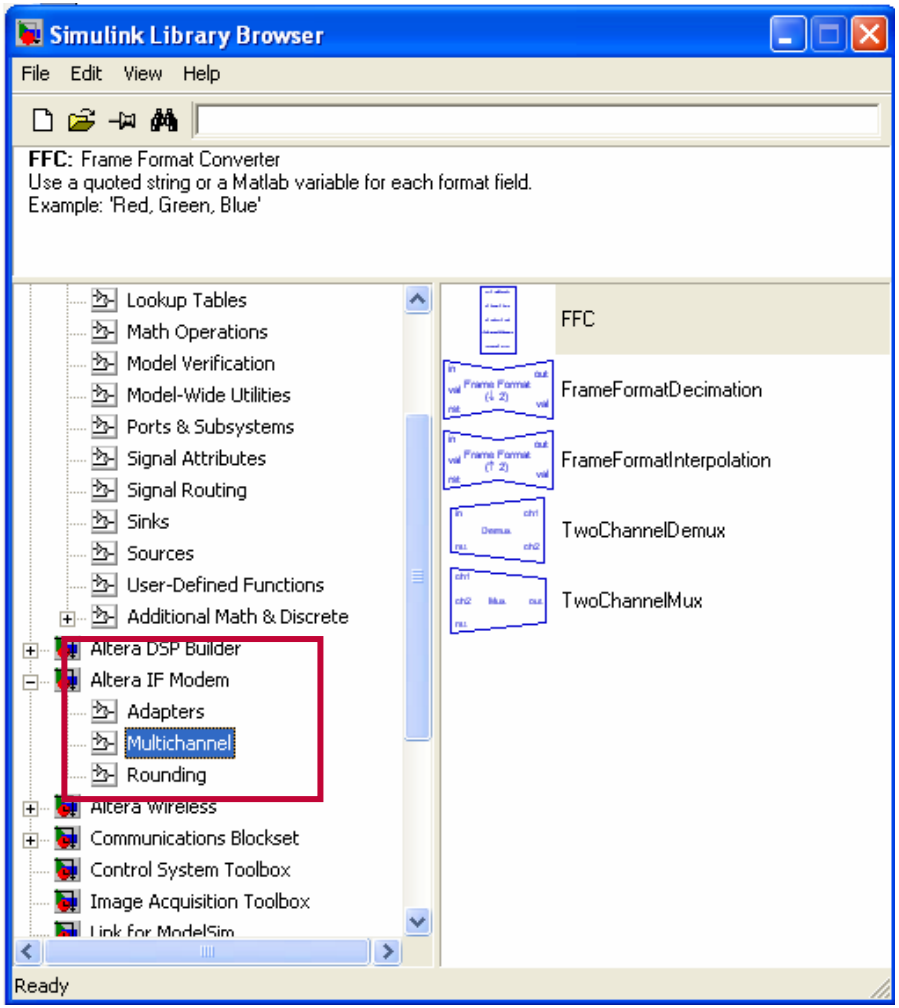
DSP Builder Implementation: IP MegaCore Library





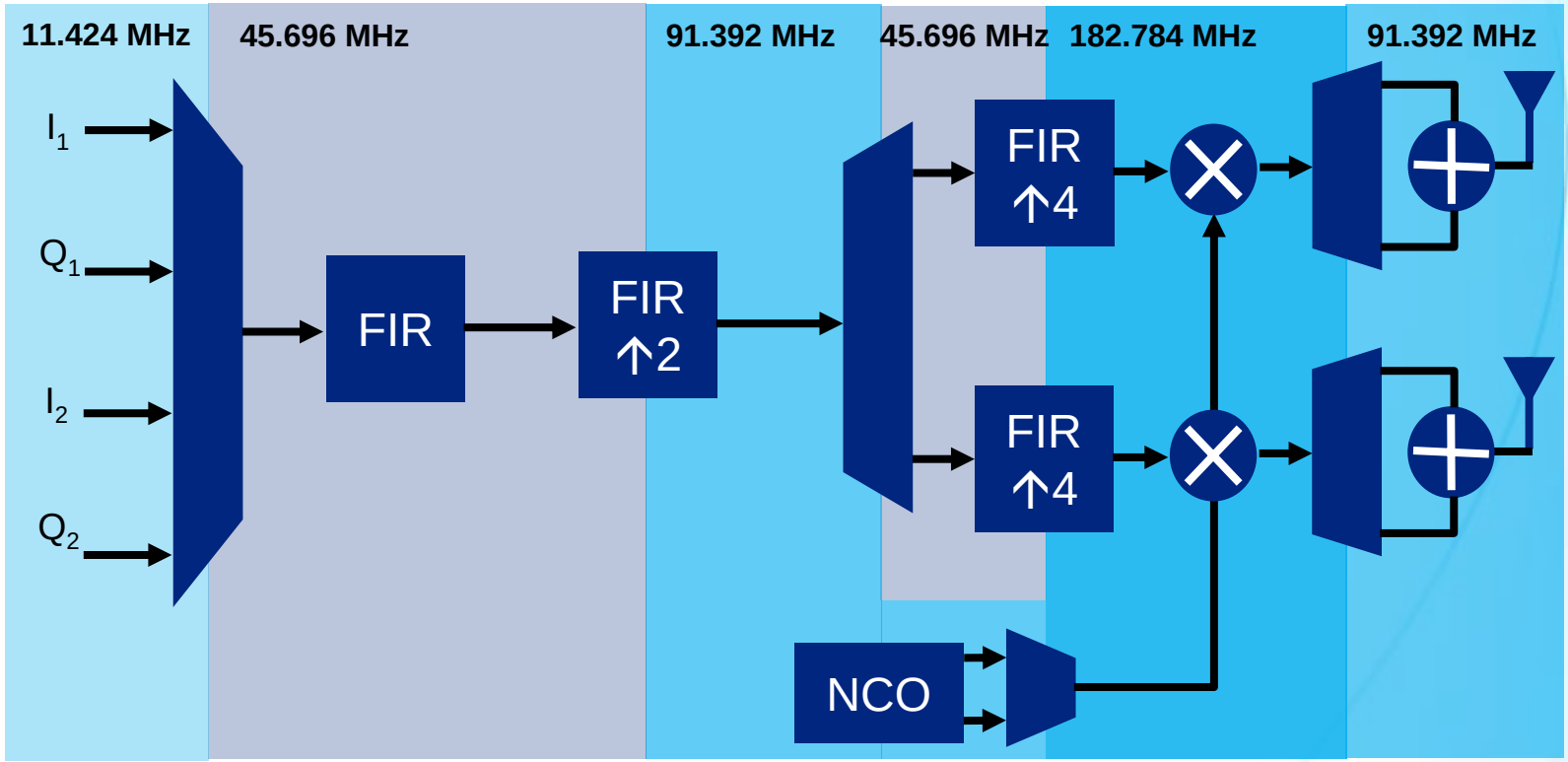
IP Can Be Added to the Library Separately

DSP Builder Implementation: Digital Intermediate Frequency (IF) Library



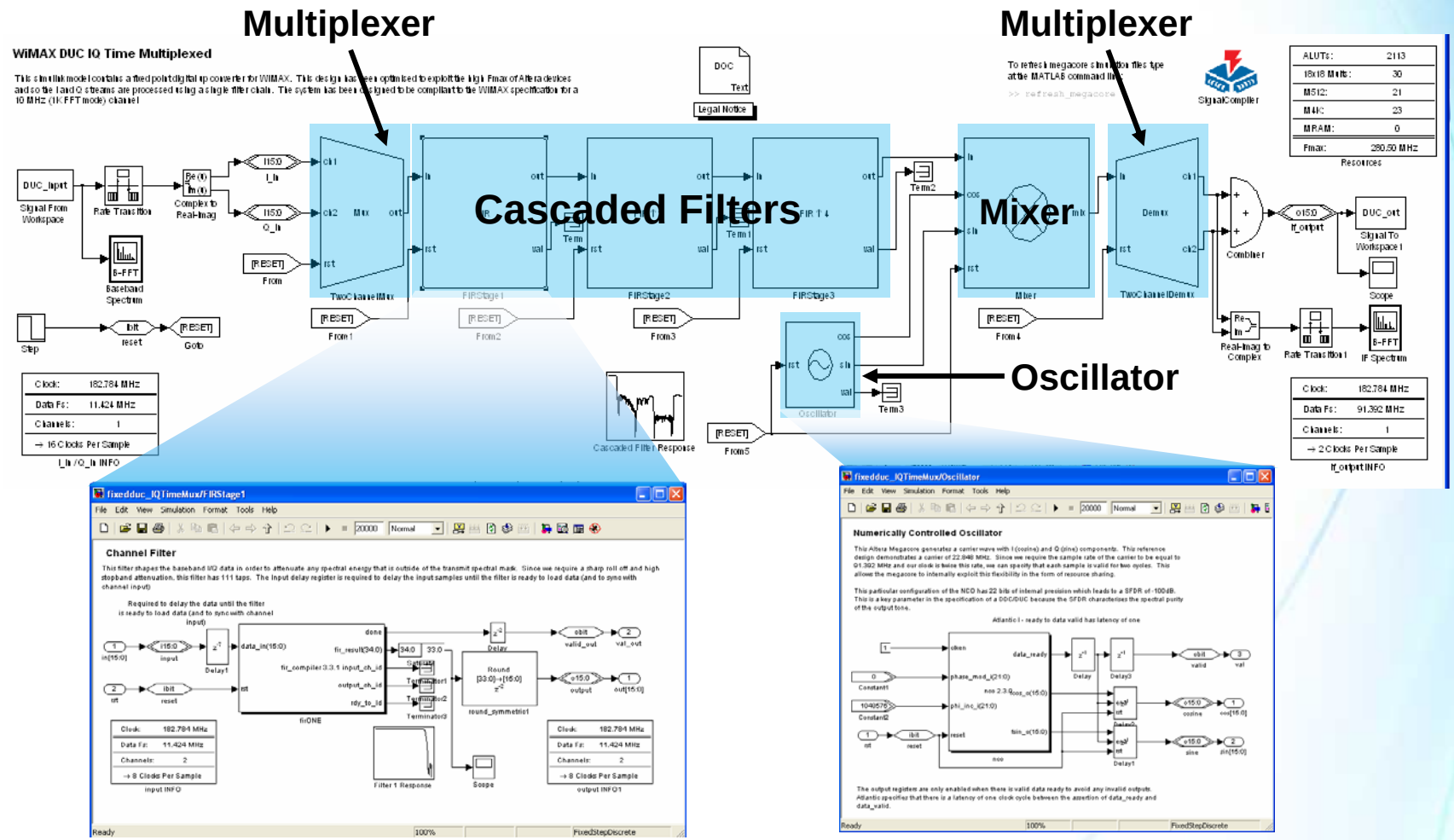
- Adapters
  - Provide input/output interface to finite impulse response (FIR) filter
- Multichannel
  - Frame format converter
  - Decimation
  - Interpolation
  - Multiplexer
  - Demultiplexer
- Rounding

DUC With 2 Antennas – Design Architecture

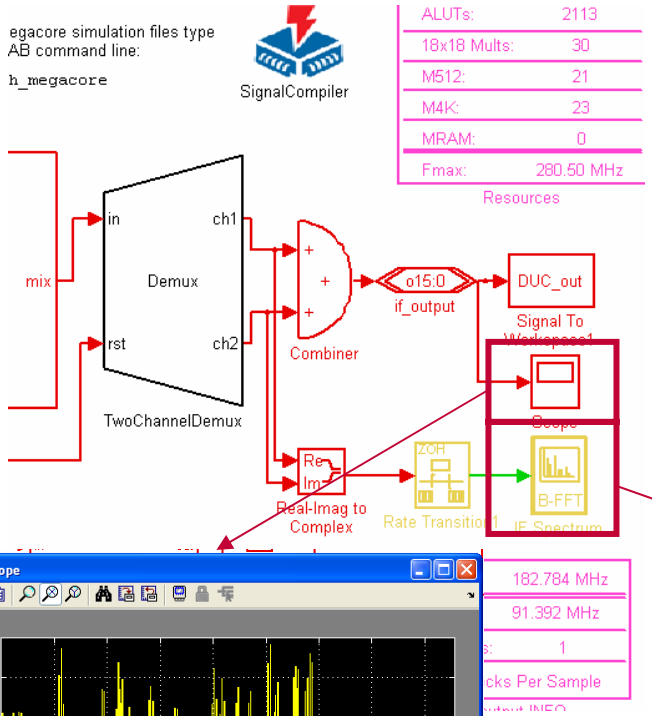


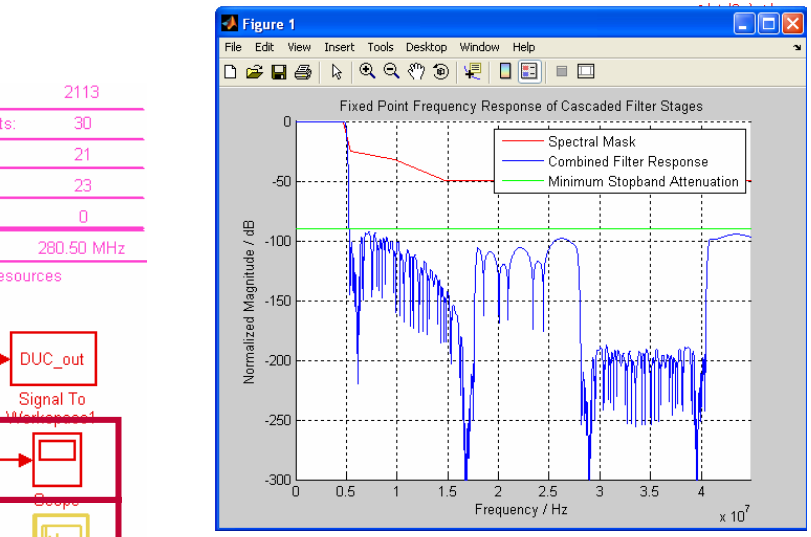
Timeshare DUC Hardware Between Antennas

DSP Builder Implementation: DUC Example Design With 2 Antennas

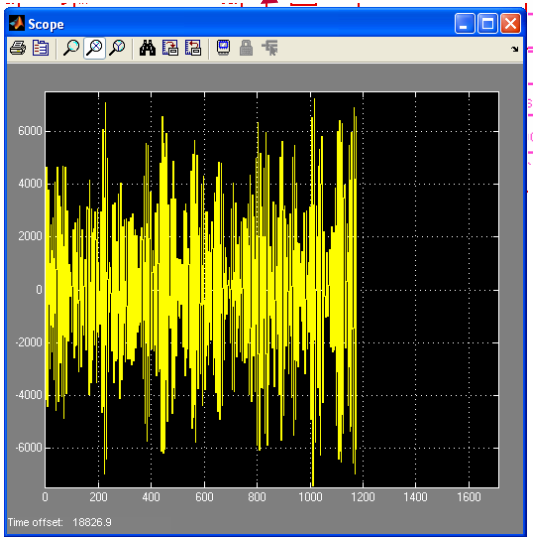


Simulation

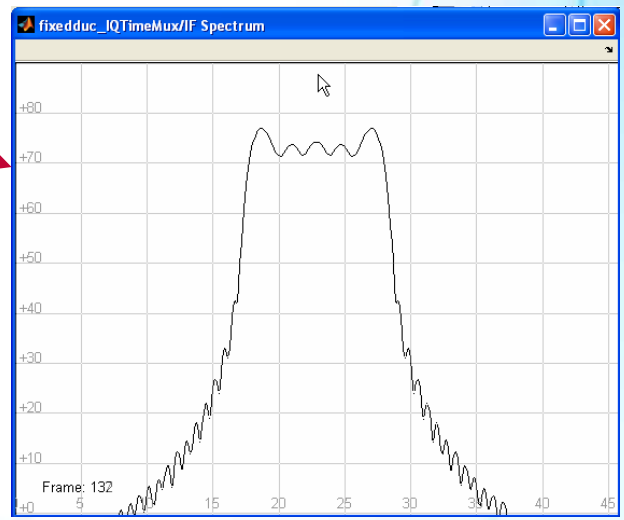




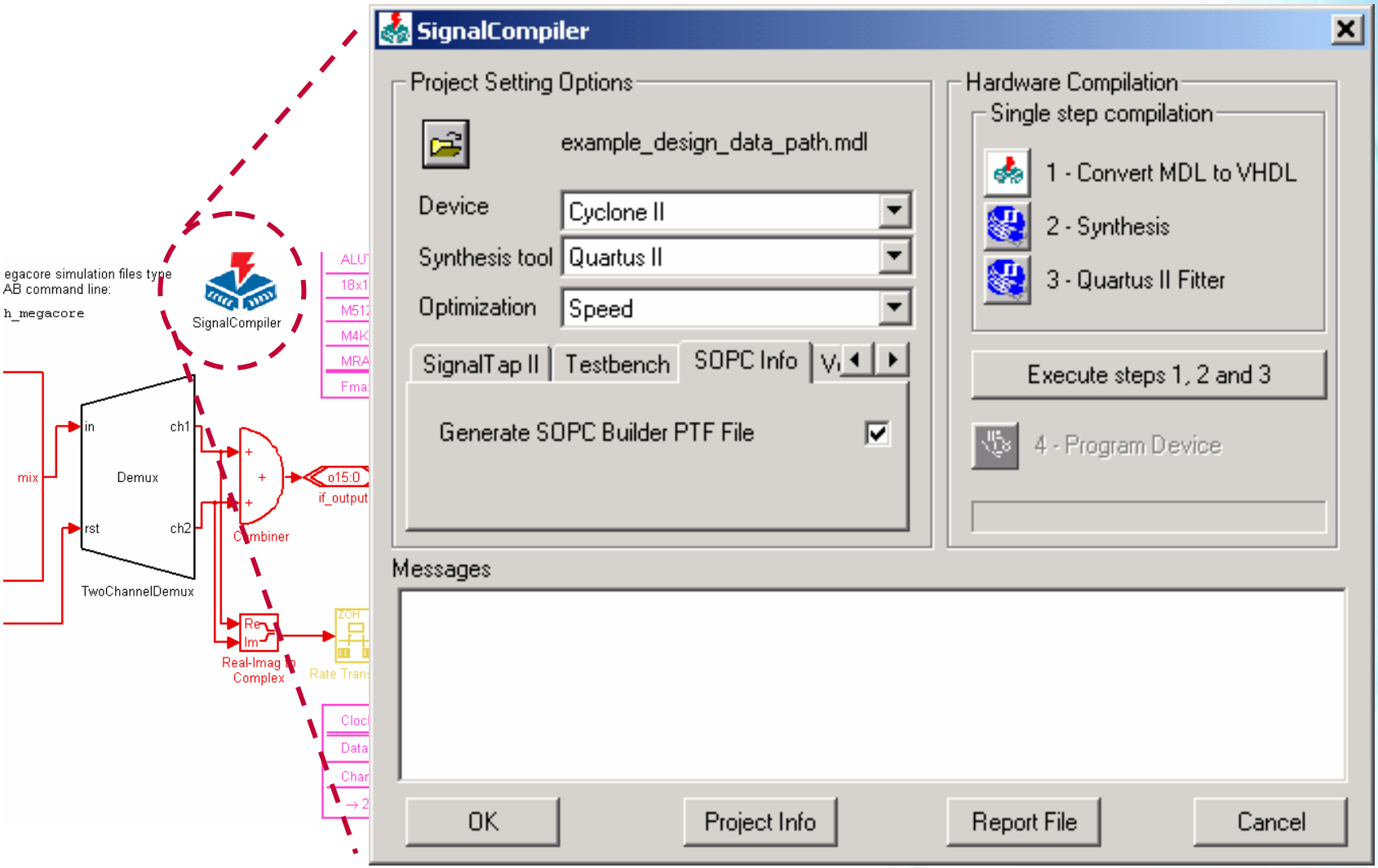
Cascaded Filter Output



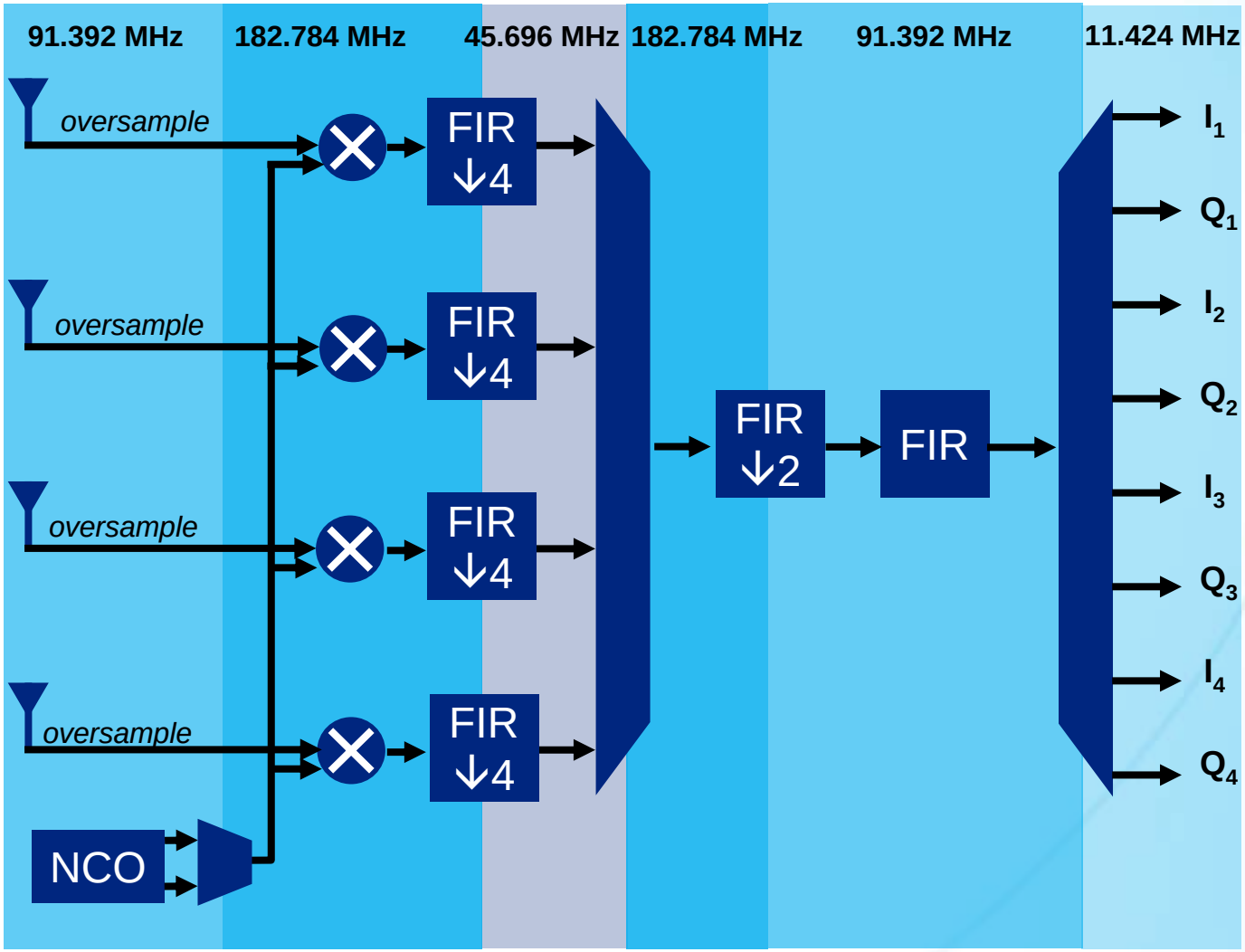
After Upconversion



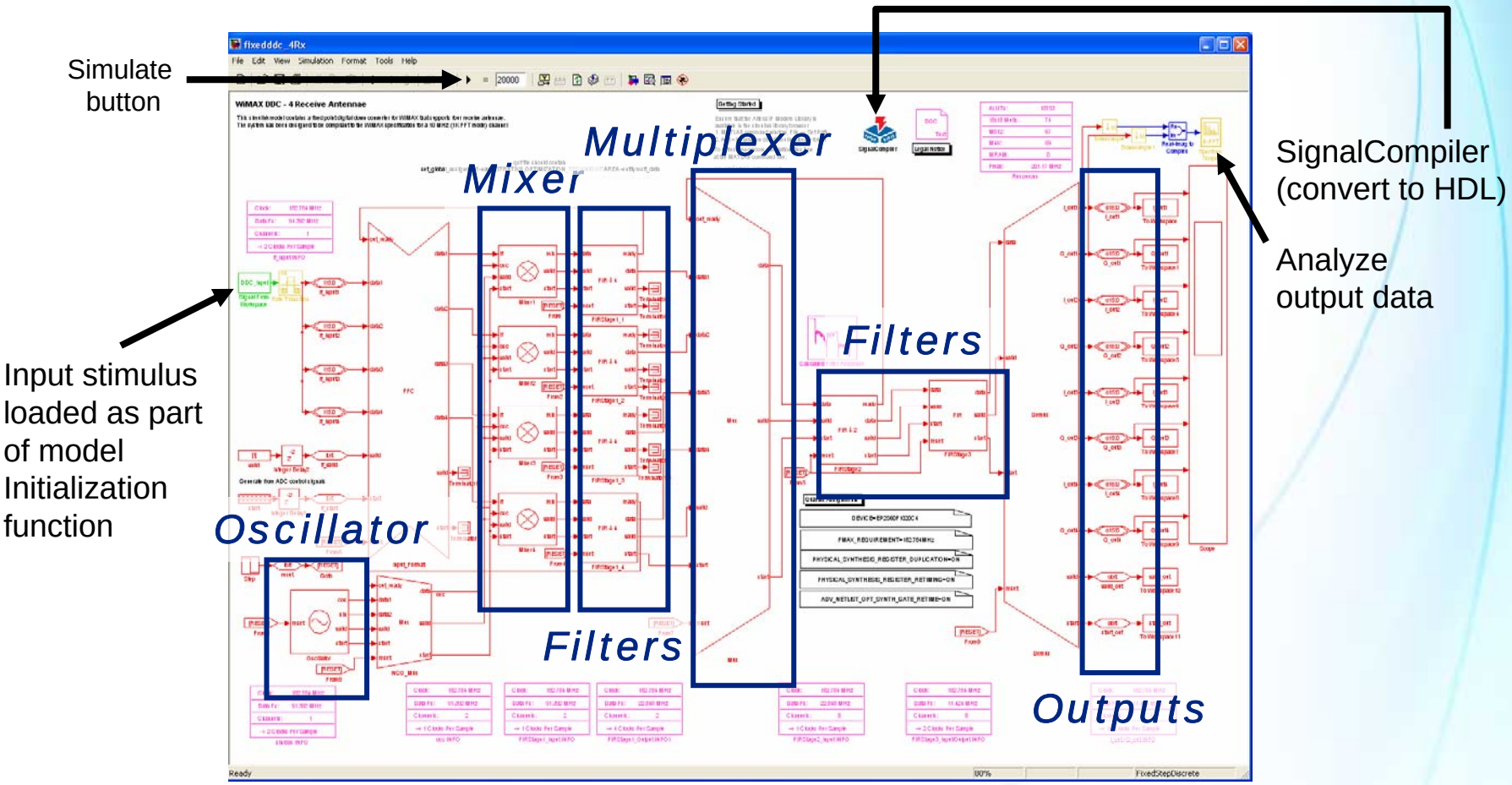
Convert to VHDL: SignalCompiler



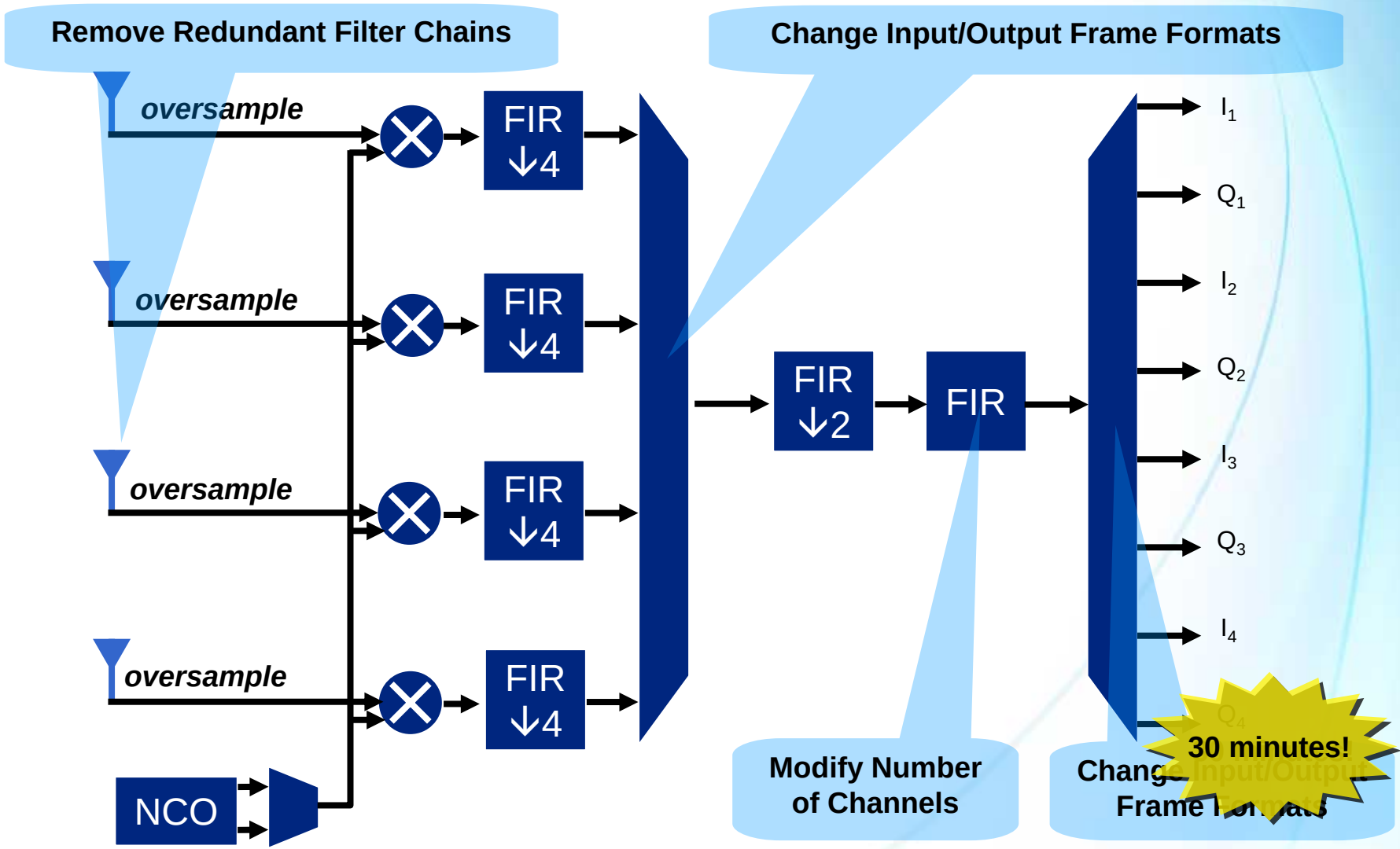
DDC With 4 Antennas – Design Architecture



DSP Builder Implementation: DDC Example Design With 4 Antennas



2xRx DDC Architecture



DUC and DDC Synthesis Results

Adaptive look-up tables (ALUTs)	M512	M4K	MRAM	Multipliers 18x18	f_{max} MHz
DUC Time Multiplexed IQ Design					
2,113	21	23	0	30	281
DUC 2 Antenna Design					
4,229	21	56	0	55	193
DDC Time Multiplexed IQ Design					
2,488	19	22	0	25	293
DDC 4 Antenna Design					
10,753	67	69	0	74	201

Highly Optimized and Cost Efficient Designs!
More Information at www.altera.com