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Implementing DSP Algorithms in PLDs

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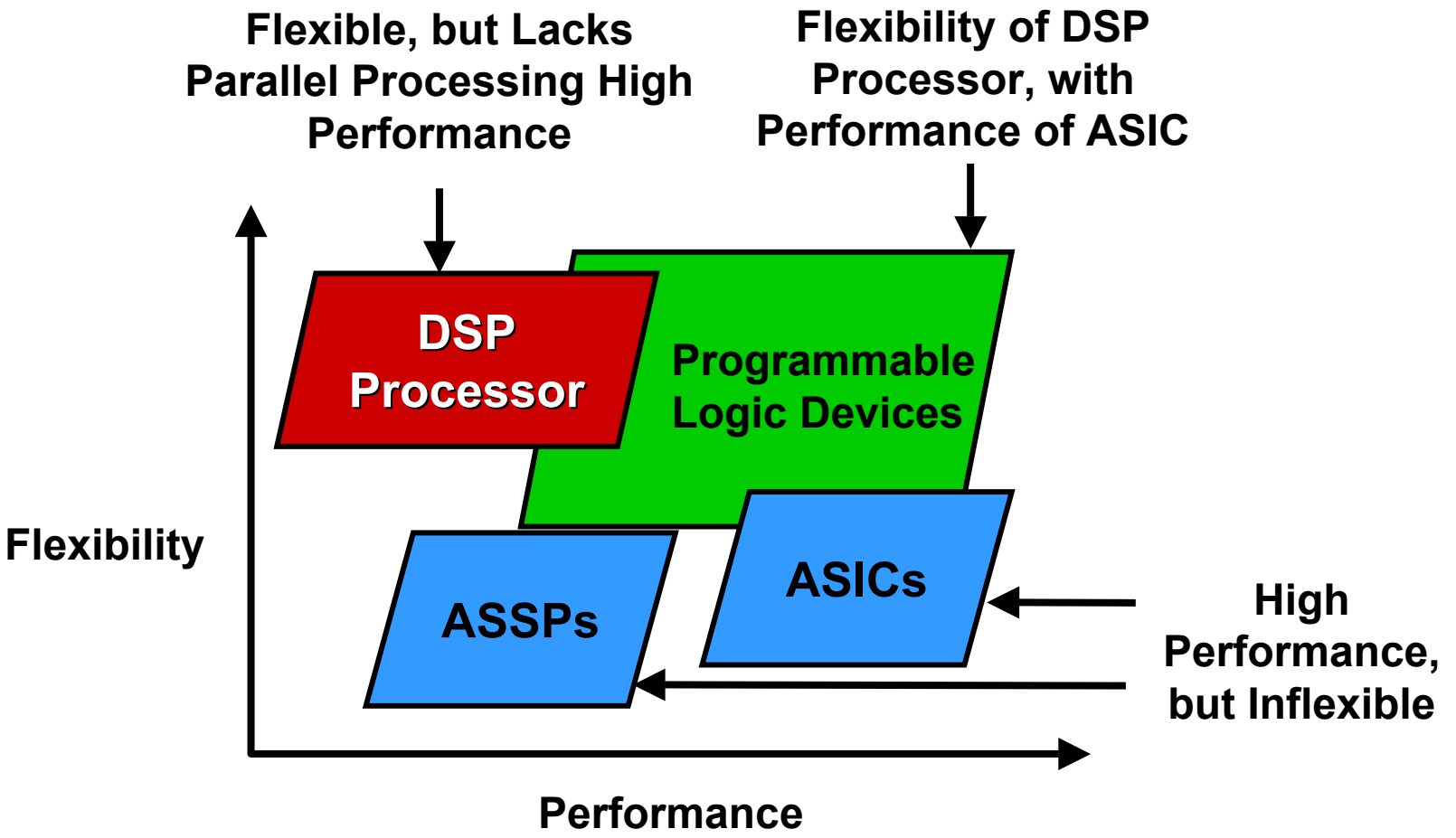
Why Use Programmable Logic Devices for DSP Applications?



High DSP Bandwidth Applications

- DSP Processors Can Address Most Single Channel DSP Applications
  - Wireless (Cell Phones)
  - Video Processing
  - Audio
- Multi-Channel Aggregation Functions Require Much Higher Bandwidth
  - VoIP – Echo Cancellation
  - Wireless Base Stations
- Critical Requirement for Multi-Channel Applications is Cost per Channel

High Bandwidth DSP Example

- Application: Terrestrial Digital Broadcasting
  - Uses Complex 1024 Tap Filter
- Requirements:
  - 4 Multiplications (16x16) per Data Sample
  - Total Multiplications = 4 * 1,024 = 4,048
  - 4 MHz Operation
- Time Division Multiplexing (TDM)
  - TDM by 32 (256 MHz)
  - Reduces Number of Multipliers Required to 64
    - Equivalent to 16,192 Multiplier MIPs

Typical Structures in DSP Algorithms

Category	Multipliers	Adders	Delay Lines
Filters: FIR, IIR, CIC	X	X	X
Transforms: FFT, DCT, DST	X	X	
Other: ECC, NCO	X	X	X

Most DSP Functions Have Multiply/Add Functionality

Bandwidth = Number of Multiplies per Time

Increasing Bandwidth

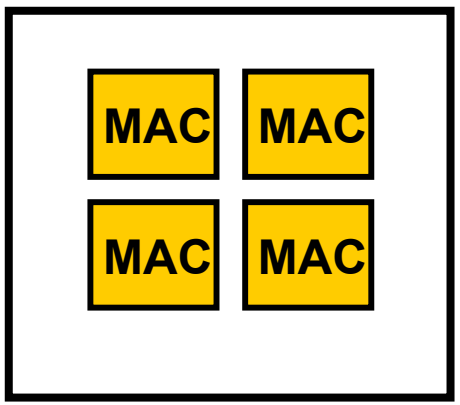
- Faster Multiplication/Add Performance
- More Multiplication/Adders in Parallel

DSP Processor Vs. FPGAs

- 1-16 Multipliers
  - Needs Looping for More than 16 Multiplications
- Needs Multiple Clock Cycles Because of Serial Computation
  - 200 Tap FIR Filter Would Need 25 Clock Cycles with 8 MACs

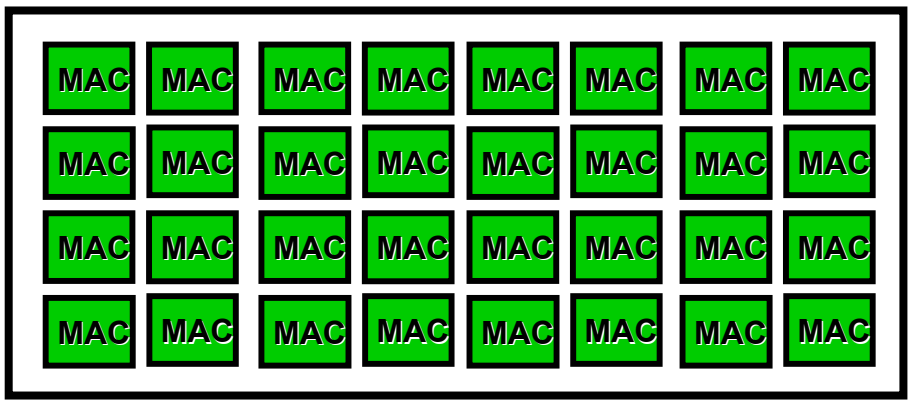
- Can Implement Hundreds of MAC Functions in an FPGA
- Parallel Implementation Allows for Faster Throughput
  - 200 Tap FIR Filter Would Need 1 Clock Cycle per Sample

High-Speed DSP Processor



Vs.

High Level of Parallel Processing

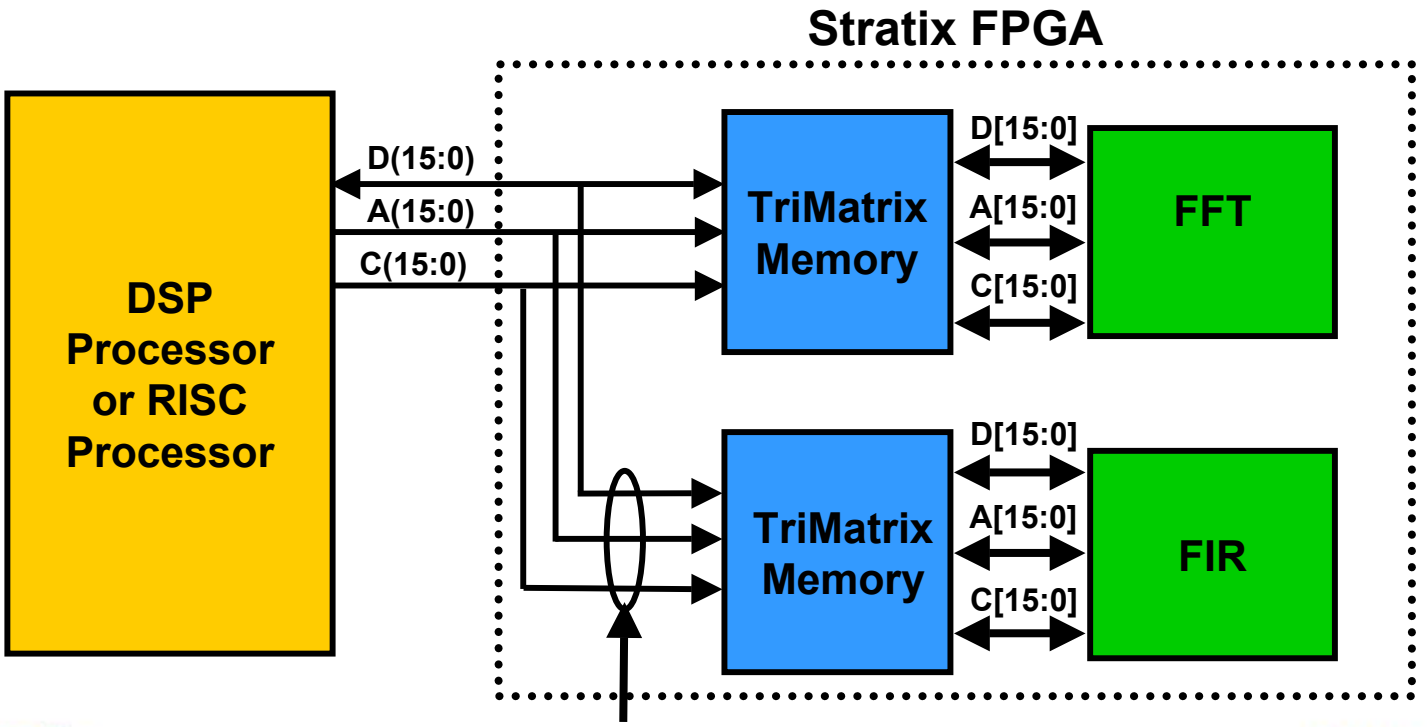


DSP Processors Vs. PLDs

Vendor	Texas Instruments	Motorola	Analog Devices	Altera
DSP Processor/ Device	TMS320C6416	MSC8102	ADSP-TS101	Stratix EP1S60
Clock Speed	600 MHz	300 MHz	250 MHz	282 MHz
Number of 16*16 Multipliers	4	16	8	72 Hard Multipliers
Multipliers MIPS	2,400	4,800	2,000	20,304
Chips Required for 1024 Tap Fir Filter	7	4	9	1

PLD for Hardware Co-Processing

- SOPC Builder Creates Avalon Interfaces
- Use of TriMatrix™ Memory as Bridge
- C to HDL Design Flow



Multipliers Options in FPGAs

Option	Resource	Area Usage	Optimal Usage
Hard Multipliers	DSP Blocks	4 - 18x18 Multipliers per DSP Block	High Speed DSP Processing
Logic Multipliers	Logic Elements	500 Logic Elements per 18x18 Multiply	Very Small Multipliers (Less than 6x6)
Soft Multipliers	Embedded RAM Blocks	1 to 2 Embedded Memory Blocks per Multiply	Complement to Hard Multipliers for Very High Bandwidth Applications

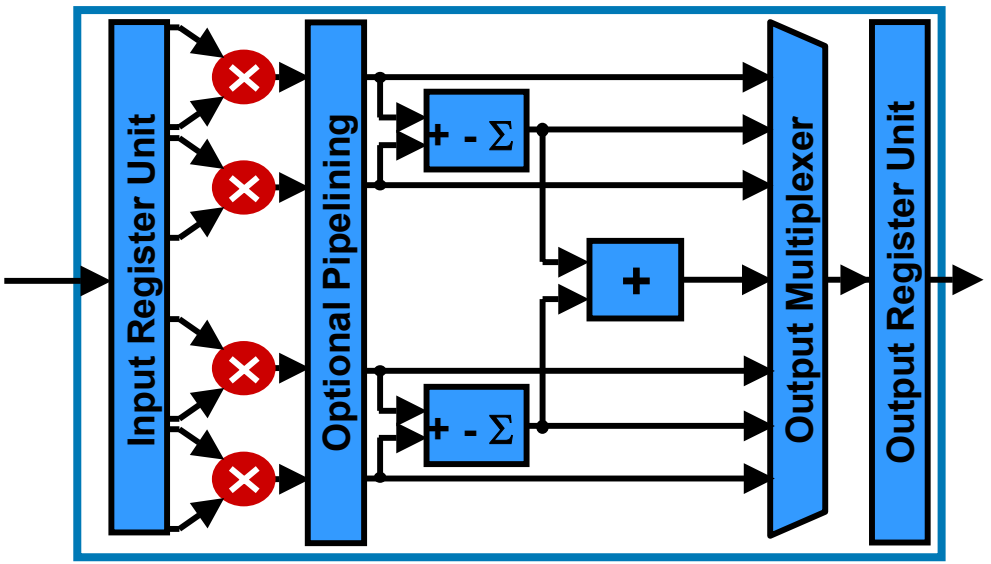
Multipliers Implementation Options

Category	DSP Blocks	Logic Elements	Soft Multipliers
Fixed Coefficient Multiplication	Yes	Yes	Yes
Variable Coefficient Multiplication	Yes	No	Yes(1)
Efficiency of FPGA Resources	High	Low	High
Flexibility	Low	Very High	High

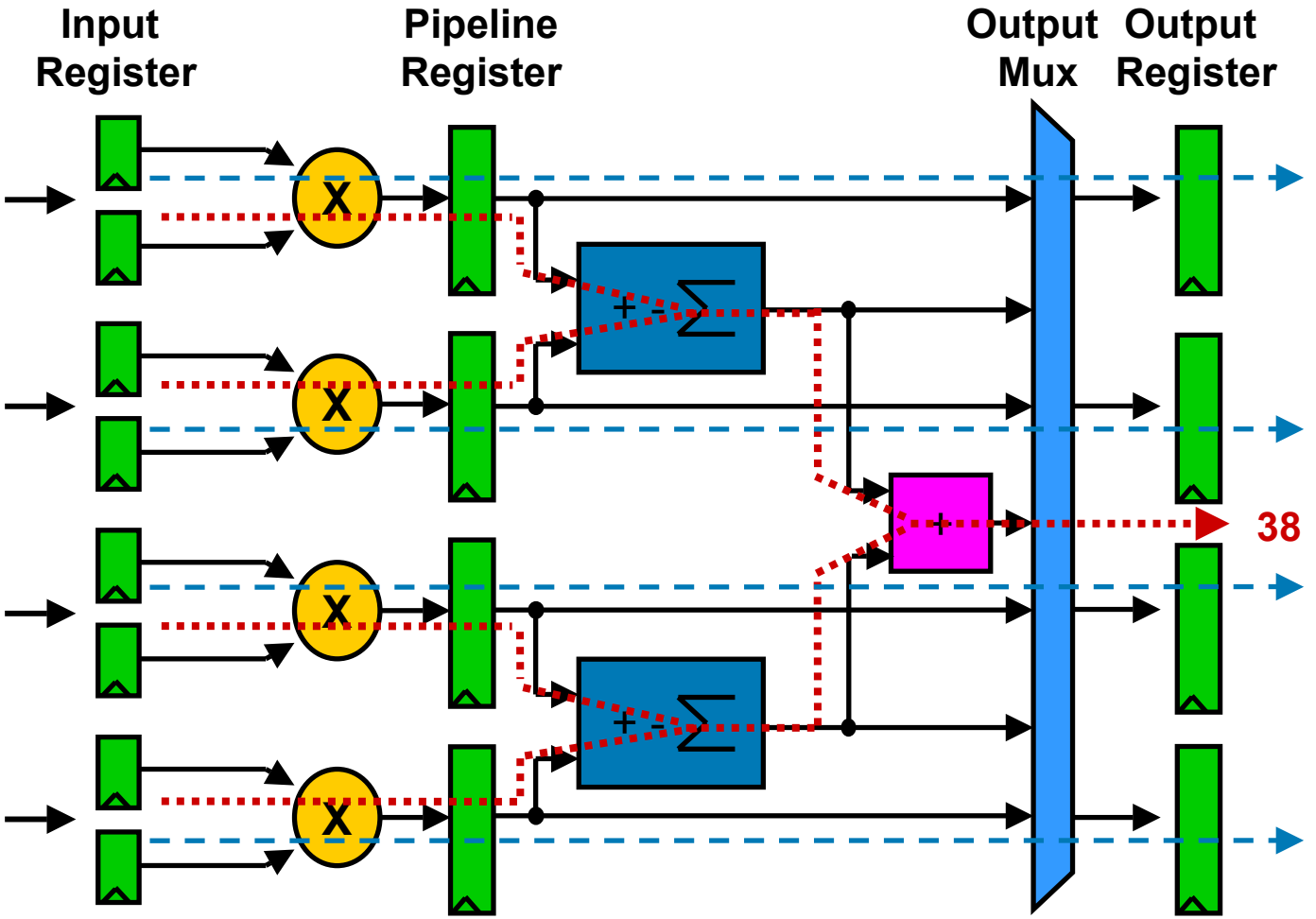
(1) Soft Multipliers Useful for Cases of Variable Coefficients When the Coefficients Update Rate Requirement Gives Enough Time to Load New Coefficients

Stratix DSP Blocks

- High Performance DSP Operation
  - 18x18 Functions at 280 MHz
- Variable Operand Widths with Full Precision Outputs
  - 9x9
  - 18x18
  - 36x36
- Add, Accumulate or Subtract
  - Signed & Unsigned Operations
  - Dynamically Change between Add & Subtract
  - Supports DSP Requirements Including Complex Numbers



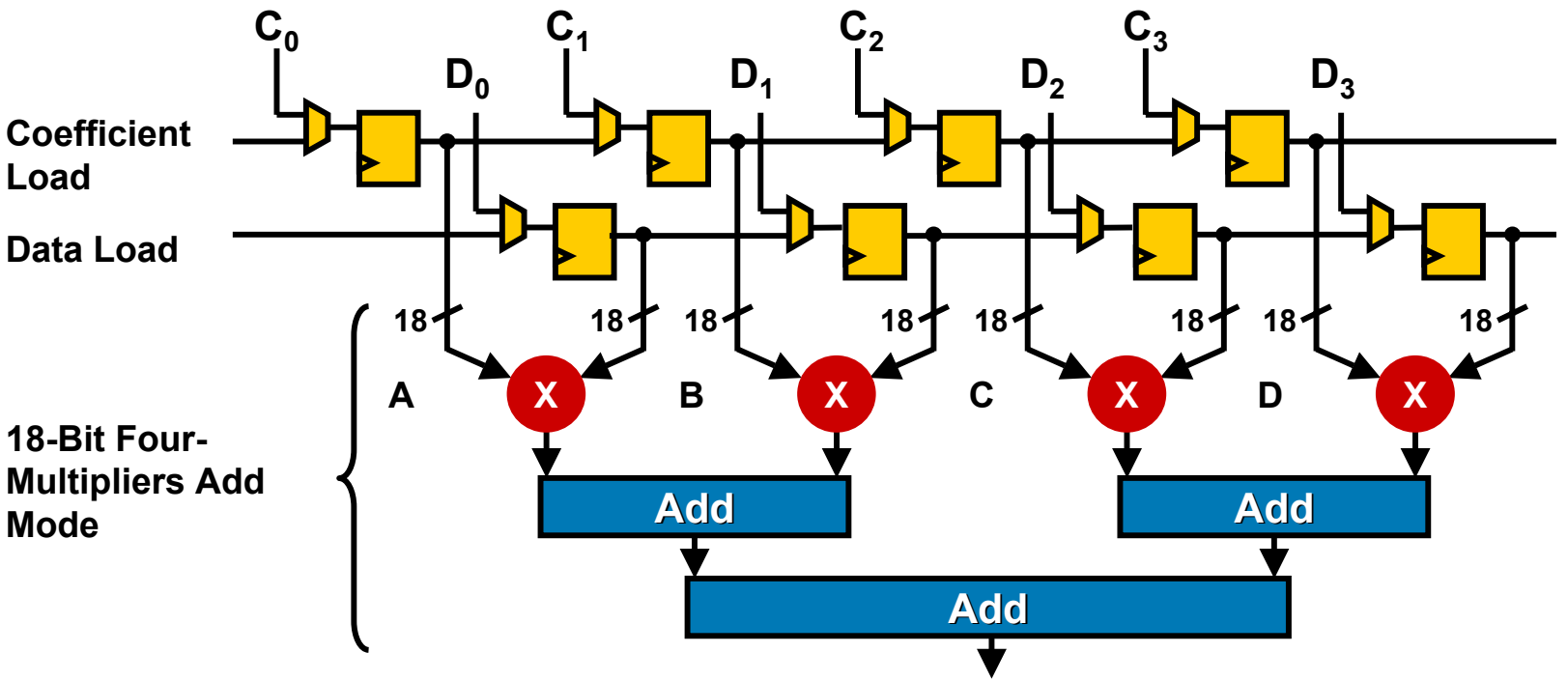
Four Multipliers Adder (18x18)



Built in Support for 4 Tap Variable FIR Filter !

DSP Block Application
4-Tap FIR Filter

- Two 18-Bit Parallel Input Shift Registers
- Implemented Entirely in Single DSP Block



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Soft Multipliers

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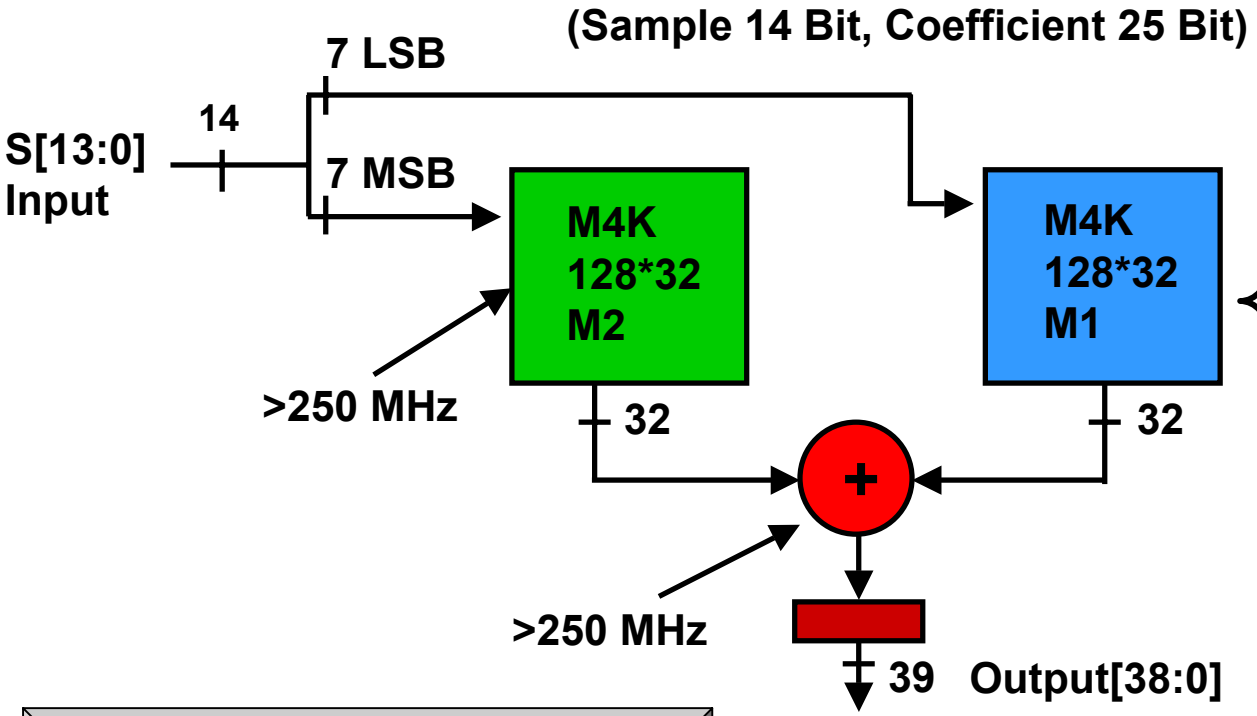
Soft Multipliers

- Use Embedded RAM Blocks for Generating Partial Products
- Address Lines Used for One Operand Input
- Coefficient or Sum of Coefficients Values Stored in RAM Blocks
- MSB Partial Product Shifted & Added to LSB Partial Product

Parallel Multiplier



Sum of Multiplications Table

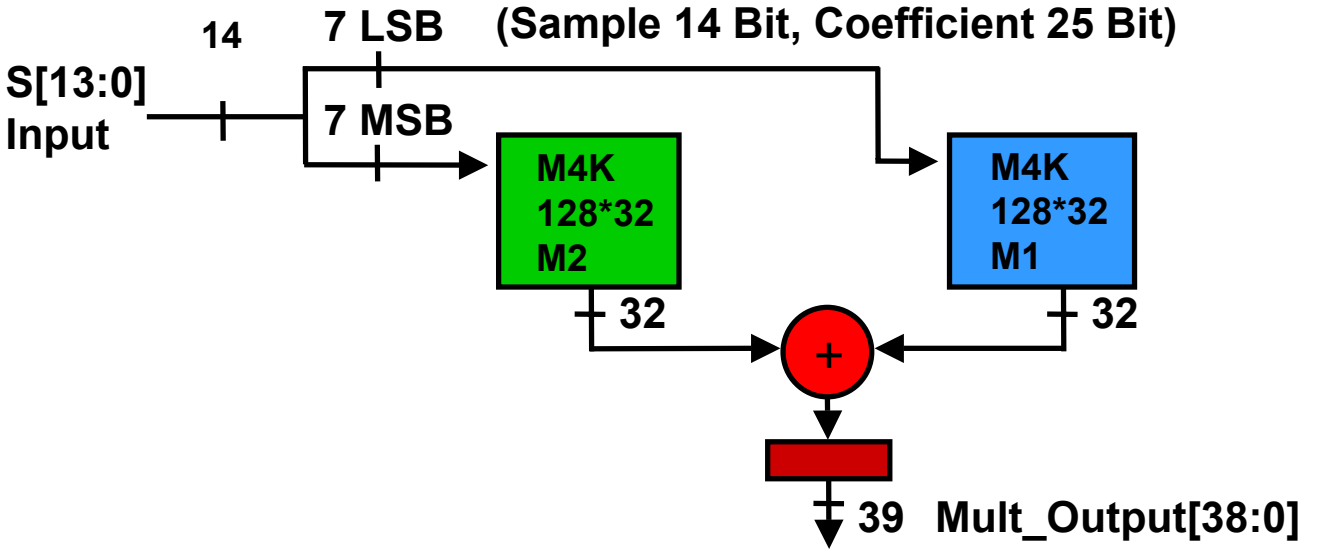
ADDRESS	MULT_RESULT
0000000	0
0000001	C
0000010	2*C
0000011	3*C
…	….
1111111	127*C

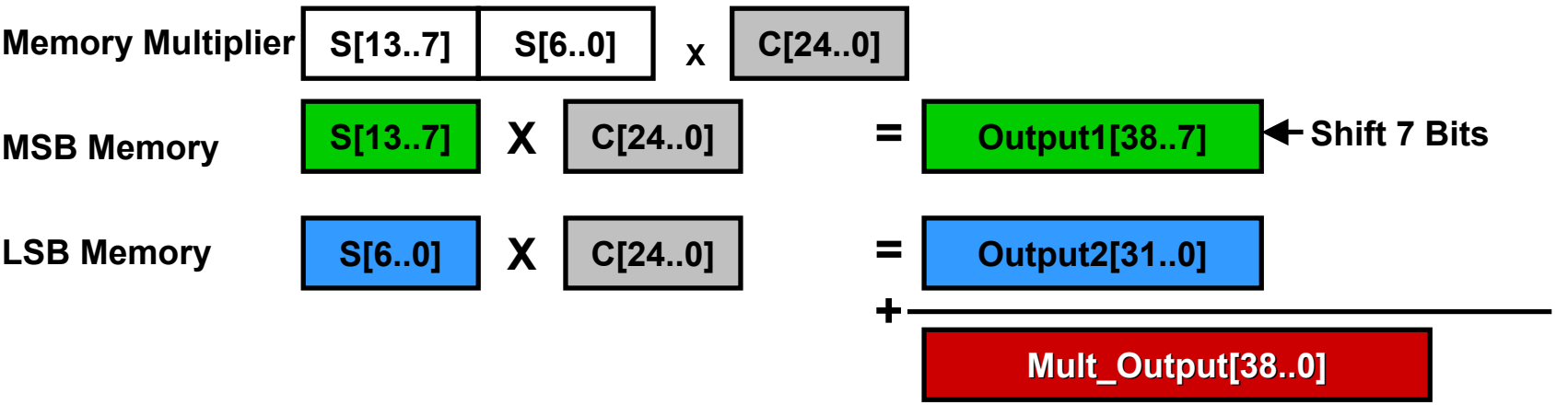
C = Coefficient[24:0]

Example: FFT Transform

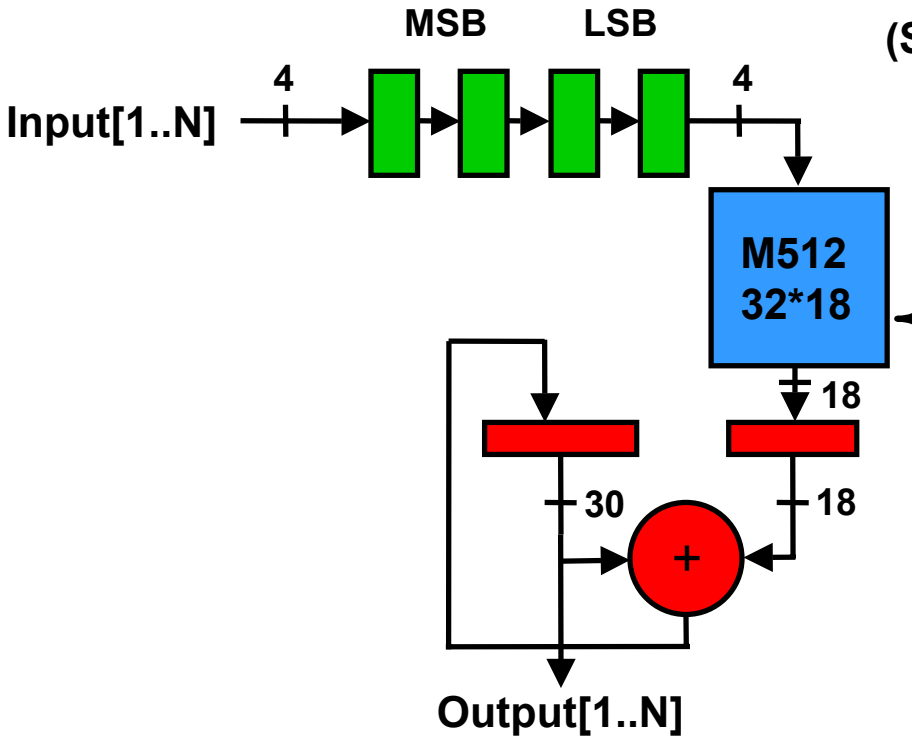
- f_{MAX}: 250 MHz
- Memory: (2) M4K Blocks
- Logic: 39 LEs

Parallel Multiplier





Semi Parallel Multiplications



(Sample 16 Bit, Coefficient 14 Bit)

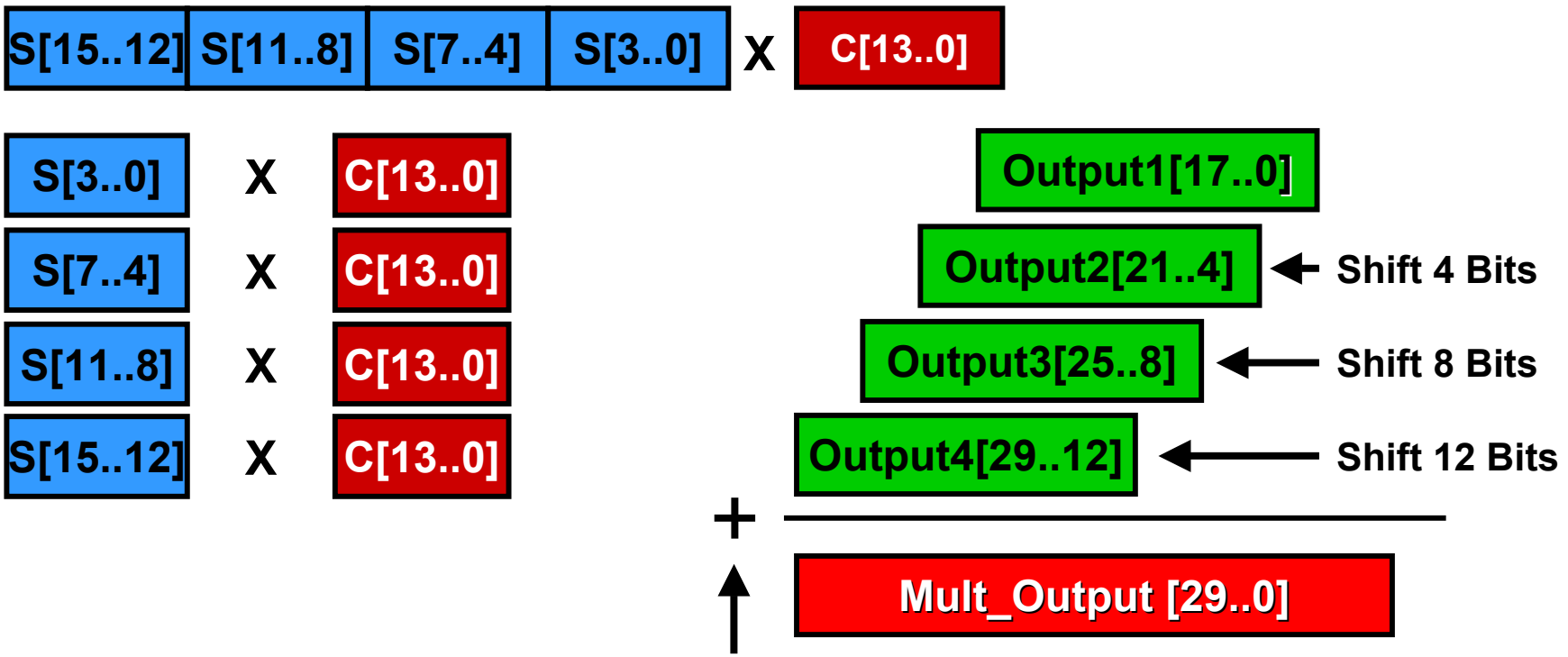
Sum of Multiplications Table

ADDRESS	MULT_RESULT
0000	0
0001	C
0010	2*C
0011	3*C
…	….
1111	15*C

Example: Equalizer

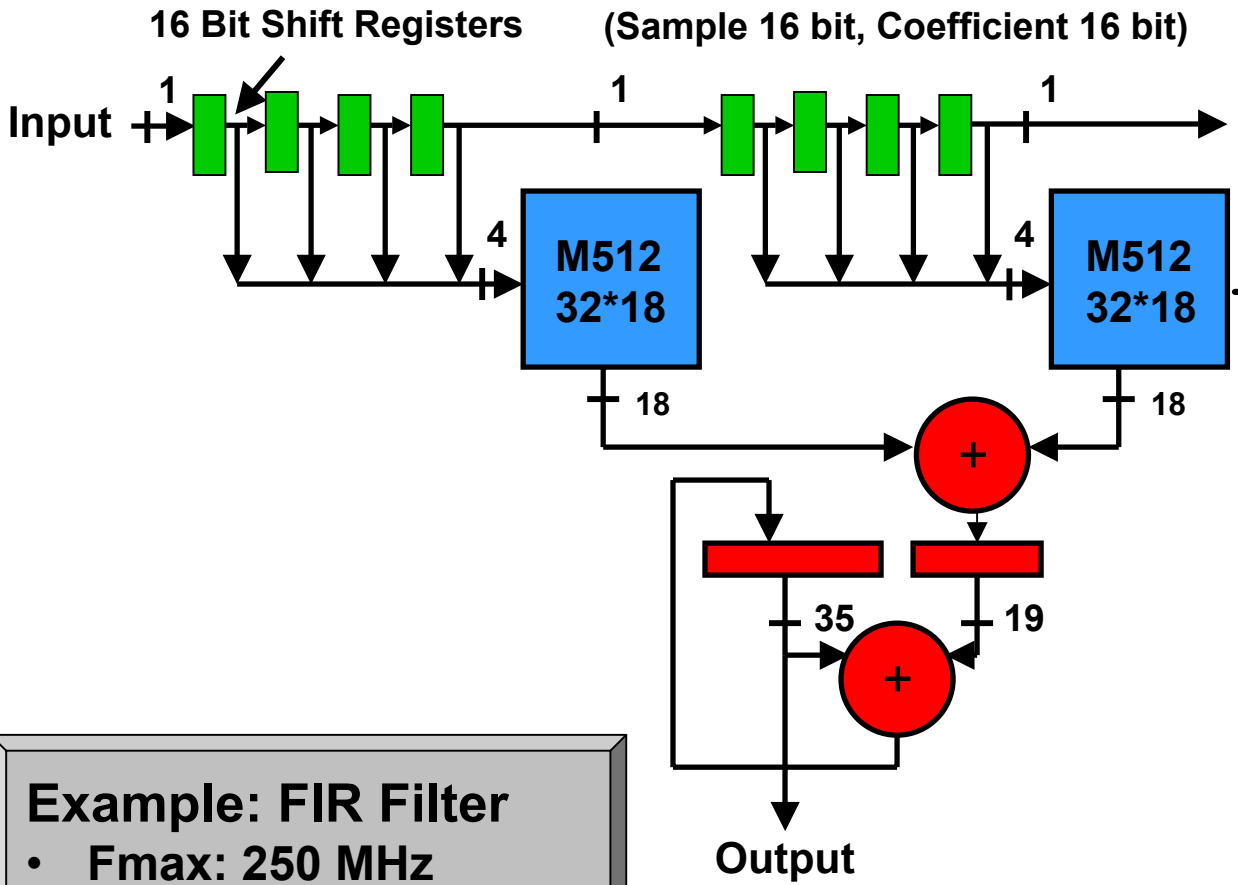
- Fmax: 250 MHz
- Memory: (1) M512 Block
- Logic: 30 LEs

Independent Multiplications



Accumulate Results from Each Multiply

Sum of Multiplications



Sum of Multiplications Table

ADDRESS	MULT_RESULT
0000	0
0001	C0
0010	C1
0011	C0+C1
…	….
1111	C0+C1+C2+C3

Example: FIR Filter

- Fmax: 250 MHz
- Memory: (2) M512
- Logic: 35 LEs

DSP Functions for Soft Multipliers

Category	Applications	Typical Memory Resources per Multiplier	Clock Cycles
Parallel	FFT, NCO, High Speed Data Scaling	Multiple	Single
Semi Parallel	Coefficients update of: LMS, Equalizer	Single	Multiple
Sum of Multipliers	FIR, DCT	Single	Multiple

The Stratix Device Family

Device	Logic Elements	32x18 M512 Blocks	128x36 M4K Blocks	DSP Blocks	16x16 Hard Multiplier	16x16 Soft Multiplier
EP1S10	10,570	94	60	6	24	53
EP1S20	18,460	194	82	10	40	89
EP1S25	25,660	224	138	10	40	125
EP1S30	32,470	295	171	12	48	158
EP1S40	41,250	384	183	14	56	187
EP1S60	57,120	574	292	18	72	289
EP1S80	79,040	767	364	22	88	373
EP1S120	114,140	1,118	520	28	112	539

DSP Processors Vs. PLDs

Vendor	Texas Instruments	Motorola	Analog Devices	Altera	Altera
Device	TMS320C6416	MSC8102	ADSP-TS101	Stratix EP1S60	Stratix EP1S10
Clock Speed	600 MHz	300 MHz	250 MHz	282 MHz	250 MHz
Number of 16*16 Multipliers	4	16	8	40 Hard	24 Hard 53 Soft
Multipliers MIPS	2,400	4,800	2,000	20,304	19,250
Number of Chips for 1024 Tap FIR Filter	7	4	9	1	1
Device Price	$202(1)	$181(2)	$196(3)	$2,380(4)	$170(4)

(1) Quoted from North American Distributor for 1K Units
(2) Press Release for 10K Units
(3) Press Release for 10K Units
(4) Altera 1K Units Price

Conclusion

- New Applications Emerging that Require Very High Bandwidth DSP Functionality
  - Optimal Solution Has Many Parallel Multiply Functions
  - Programmable Logic Is the Lowest Cost Solution for These Applications
- Stratix Has the Largest Single Chip DSP Parallel Processing Capability
  - DSP Blocks
  - Soft Multipliers