(Technical)

Document No.: MJL-LD-AN-3
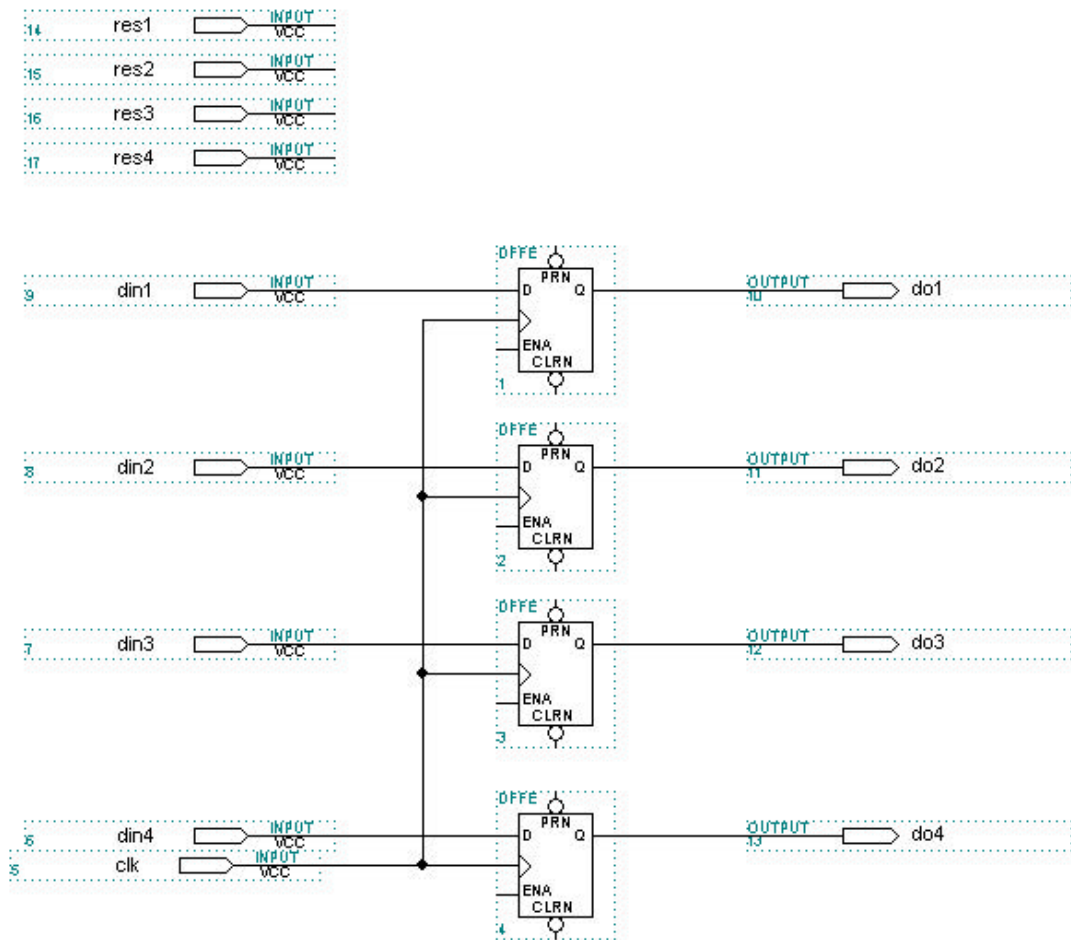
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Version: 1.0

Date: 2000 3 23

Subject: **Design** - (reserved pins)

Altera Device

1 Pin Assignment

1.   .

    Used Pins :   .

    Unused Pins :   .

    Reserved Pins :   .

                    EPF6016AQC240-3   .

                    compile (place and route)   Altera software   MAX+plus II
                    PQFP240 package   .

Report File   .

```
** DEVICE SUMMARY **
Chip/                    Input   Output  Bidir                          LCs
POF      Device        Pins    Pins    Pins    LCs    %Utilized

reserved_pins
      EPF6016AQC208-3    5       4       0       4         0 %

User Pins:              5       4       0
Project Information                        c:\mywork\reserved_pins.rpt
** PROJECT COMPILATION MESSAGES **
Warning: Ignored unnecessary INPUT pin 'res4'
Warning: Ignored unnecessary INPUT pin 'res3'
Warning: Ignored unnecessary INPUT pin 'res2'
Warning: Ignored unnecessary INPUT pin 'res1'
Device-Specific Information :            c:\mywork\reserved_pins.rpt
reserved_pins
** INPUTS **
                                    Fan-In   Fan-Out
 Pin   LC  Row Col  Primitive   Code  INP FBK  OUT FBK  Name
  24    -   -   --    INPUT     G.    0   0    0   0   clk
 205    -   A   --    INPUT           0   0    0   1   din1
 206    -   A   --    INPUT           0   0    0   1   din2
 207    -   A   --    INPUT           0   0    0   1   din3
 208    -   A   --    INPUT           0   0    0   1   din4
** OUTPUTS **
        Fed By                      Fan-In   Fan-Out
 Pin   LC  Row Col  Primitive   Code  INP FBK  OUT FBK  Name
   1    -   A   --    OUTPUT    $     0   1    0   0   do1
   3    -   A   --    OUTPUT    $     0   1    0   0   do2
   2    -   A   --    OUTPUT    $     0   1    0   0   do3
 204    -   -   O1    OUTPUT    $     0   1    0   0   do4
```

                  PCB   24   , 205 , 206 , 207 , 1 , 3 , 2 , 204
                      PCB   report file   PQFP240
                                      reserved pin   ,
PCB   no connection   .

                              .

53 , 54 , 55 , 56

PCB ?

, CHIP

. ?

.

MAX+plus II software compile chip GND
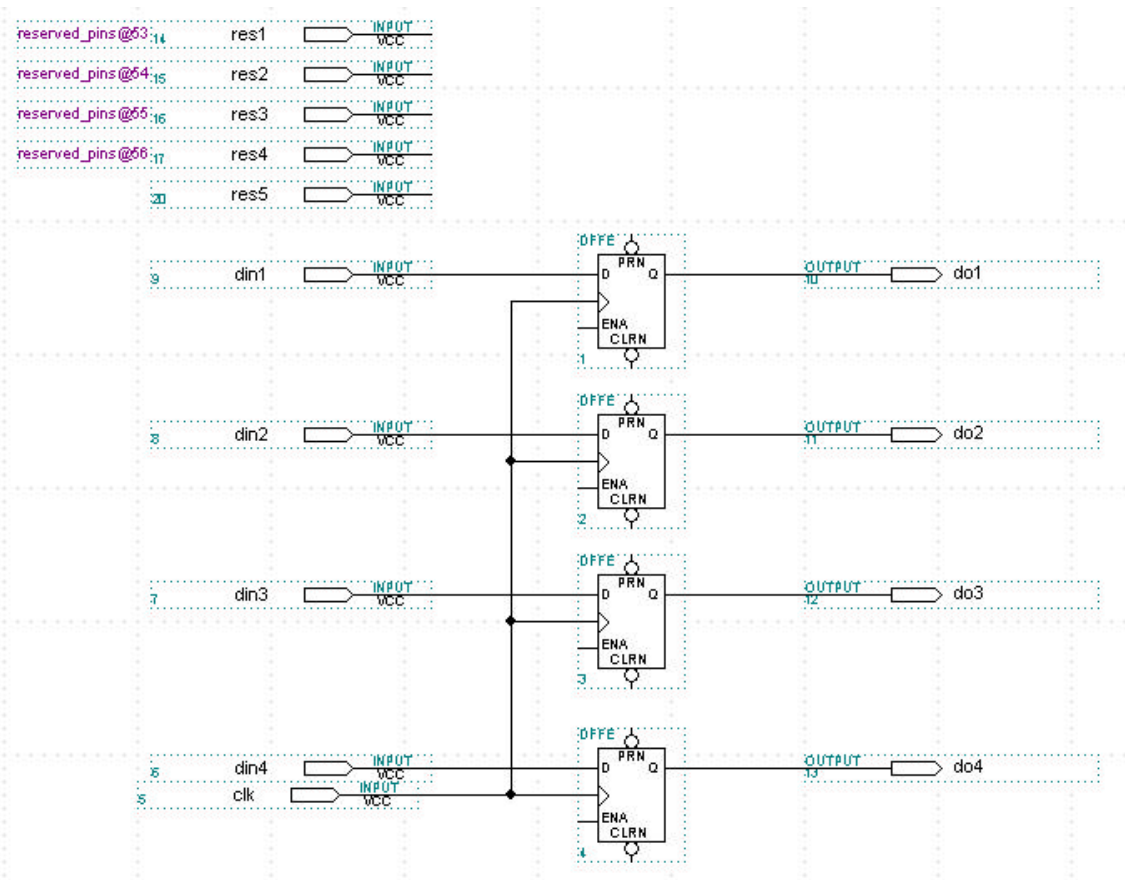. ? PCB pattern
PCB ground plane .
Altera Chip ground .
.

?
PCB FPGA
?

res1, res2, res3, res4, res5 (FPGA
) PCB
, MAX+plus II ?

INPUT, OUTPUT SYMBOL MOUSE
ASSIGN Pin/Location/Chip... Pin/Location/Chip
.

:

, Device
Target Device **Pin** **.**

.

reserved_pins@63 14 res1 INPUT VCC

reserved_pins@64 15 res2 INPUT VCC

reserved_pins@65 16 res3 INPUT VCC

reserved_pins@66 17 res4 INPUT VCC

20 res5 INPUT VCC

9 din1 INPUT VCC   DFFE PRN D Q ENA CLRN 1   OUTPUT 10 do1

8 din2 INPUT VCC   DFFE PRN D Q ENA CLRN 2   OUTPUT 11 do2

7 din3 INPUT VCC   DFFE PRN D Q ENA CLRN 3   OUTPUT 12 do3

6 din4 INPUT VCC   DFFE PRN D Q ENA CLRN 4   OUTPUT 13 do4
5 clk INPUT VCC

2 Reserved_pin Assignment

compile   report file   .

Project Information   c:\mywork\reserved_pins.rpt
** PROJECT COMPILATION MESSAGES **
Warning: Ignored unnecessary INPUT pin 'res5'
Info: Reserved unused input pin 'res4' for future use because it has a pin assignment -- pin is tri-stated and must be connected to your board
Info: Reserved unused input pin 'res3' for future use because it has a pin assignment -- pin is tri-stated and must be connected to your board
Info: Reserved unused input pin 'res2' for future use because it has a pin assignment -- pin is tri-stated and must be connected to your board
Info: Reserved unused input pin 'res1' for future use because it has a pin assignment -- pin is tri-stated and must be connected to your board

tri-state   PCB
.

Revision History

- 2000-3-23 - Ver 1.0: Initialize Release...