Fabrication Technologies for Three-Dimensional Integrated Circuits

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Abstract

The MIT approach to 3-D VLSI integration is based on low-temperature Cu-Cu wafer bonding. Device wafers are bonded in a face-to-back manner, with short vertical vias and Cu-Cu pads as the inter-wafer throughway. In our scheme, there are several reliability criteria, which include: a) Structural integrity of the Cu-Cu bond, b) Cu-Cu contact electrical characteristics, and c) Process flow efficiency and repeatability. In addition, CAD tools are needed to aid in design and layout of 3DICs. This paper will discuss recent results in all these areas.

1. Introduction

Three-dimensional integrated circuits (3DICs) have attracted attention in industry and academia as it may provide an enabling technology that relaxes today's interconnect-bottleneck. As device densities continue to increase with advances in lithography and device design, device-to-device interconnects will continue to be a major design issue. The ITRS 99 roadmap projects that the number of metal layers at the 50-nm generation will be 9-10. With current manufacturing technologies, it will be a major challenge for future designs to be able to manage such complexity while maintaining the performance improvements that the market demands. Multi-layer device structures such as 3D-ICs, are seen as a possible solution for this challenge.

It can be shown that 3-D architectures can reduce the overall global and semi-global wire-length, while increasing the number of local wires [1]. Moreover, the decrease in the number of long interconnects could directly translate to an increase in device density, provided that the devices are efficiently packed, placed, and wired. In addition to these potential benefits, the 3-D architecture lends itself to the realization of a "system-on-a-chip." Monolithic mixed-technology options, such as 3-D imagers, have already shown promise [2,3]. Other opportunities, such as OEIC-on-Si technology, memory-on-logic, and various microelectromechanical (MEMS) hybrids are also possible.

There exist a plethora of 3-D integration techniques in literature, but the two most appealing and competitive schemes to date are those involving either low-temperature silicon epitaxy or wafer bonding. The central theme between these two methods is vertical integration - namely, the addition of CMOS devices on top of each other. Their inherent differences, however, are of course the stacking technique itself, as well as each scheme's potential for high vertical connectivity and "system-on-a-chip" integration.

For instance, in the epitaxy scheme, multiple device layers can be realized by repeating the "Si epitaxy followed by a CMOS flow" cycle" [4], where successive device layers are fabricated in serial mode. The enabling technology is a well-characterized low-temperature Si epitaxy, which is crucial for thermal budget minimization of the process flow. Layer-to-layer connections can made from either inter-layer vias (as in [4]) or from direct source-drain / source-drain contacts using sandwiched polysilicon lines. In theory, the combination of Si epitaxy with local poly-Si interconnects would probably create a true 3-D system, where it will contain the highest vertical connectivity of all current 3-D schemes. But 3-D integration with serial Si epitaxy comes with a price: It will be very difficult to implement circuit integration with mixed-technologies (i.e. III-V optics with CMOS).

On the other hand, in the wafer bonding approach, integration of mixed technologies is of second nature. In most wafer bonding schemes [2,3,5,6], multiple device wafers in the stack are held together with adhesives (i.e. polymers, metal-to-metal thermocompression, low-melting point eutectic solders, etc.), and inter-layer vias provide layer-to-layer communication. Although the process flows do vary significantly, most wafer bonding schemes share four common considerations: a) The bonding medium ("glue") of choice, b) If needed, a method for Si substrate thinning, c) The wafer-to-wafer alignment accuracy, and d) The inter-layer electrical interconnection method. To be specific, the remainder of this paper will focus on these

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considerations that apply to 3-D integration with Cu-Cu wafer bonding.

2. Process Flow

In our 3-D integration scheme, multiple device wafers are sequentially bonded to each other using low-temperature Cu-Cu thermocompression. Figure 1 depicts our definition of a 3-D circuit, in which two device layers are both bonded and electrically interconnected using Cu-Cu pads (the bonding interface).

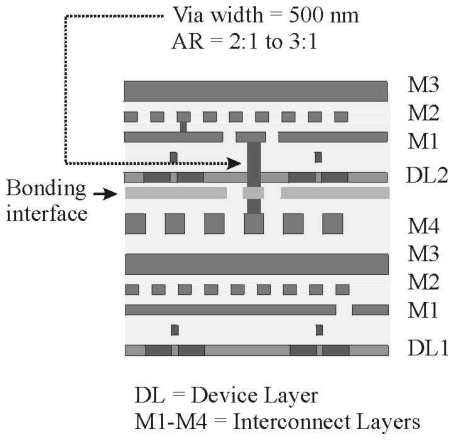

Figure 1. A typical 3-D circuit

The ideal case for such architecture is to have the smallest possible lateral dimensions for the Cu pads and inter-wafer vias to ensure high via density. In reality, wafer-wafer alignment tolerances during bonding and the maximum aspect ratio of the vias one can create will ultimately be the size-limiting determinants of these vias / Cu pads (see Section 2.3). As shown in Figure 1, when the top device layer is a thin SOI, the aspect ratio of the inter-wafer vias can be relaxed to around 3:1 or even 2:1 for ease in fabrication, while still maintaining a relatively high vertical density across the wafer.

To recapitulate, the goal of our process flow is to create a 3-D stack by successive bonding of SOI device layers on top of each other. Figure 2 is a flowchart of such a process, in which the 3-D stack begins with bonding of two device wafers, and subsequent device layers can be added to the stack in a short turn-around process loop. As seen in this chart, the majority of the processing steps revolve around the preparation of the first SOI substrate prior to bonding (mainly for substrate thinning), which is the focus of the next three subsections.

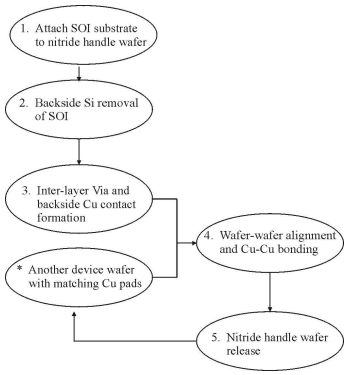

Figure 2. Process flowchart

2.1. Handle Wafer Attachment

Our 3-D scheme begins with a typical SOI substrate (100 nm SOI / 400 nm BOX) that contains both CMOS devices and its corresponding multilevel interconnects - essentially a "finished" circuit. Next, in order to stack this SOI on top of another device layer, it first has to undergo backside substrate thinning. For mechanical support during grindback, it is imperative to attach the SOI to a handle wafer with a special adhesive that is: a) Strong enough to withstand vigorous shearing force from grinding (section 2.2), b) Chemically inert to hot aqueous hydroxide solutions (section 2.2), and c) Can easily be removed with another solution (section 2.4).

Because hot basic solutions will usually delaminate organic polymers from their substrates, it is very difficult for CMOS-compatible polymer adhesives to satisfy all three criteria. However, these requirements can be met with a careful choice of metallic bonding layers; hence, one can use a Cu-Cu bond as the adhesion layer itself, while flanking layers of Zr can be used as the "wafer release" medium. This is due to the fact that Cu generally resists hydroxide attack, and Zr dissolves extremely rapidly in dilute HF (much faster than SiO_2). The complete handle wafer attachment scheme is shown below in Figure 3.

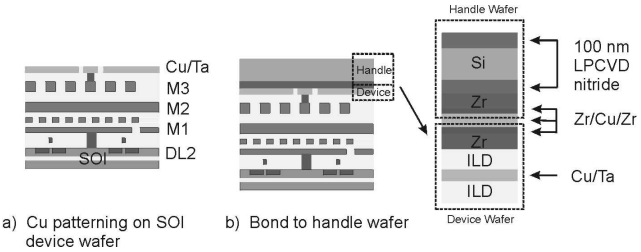

Figure 3. Handle wafer attachment of SOI substrate

To begin with, (300 / 50) nm thick Cu/Ta contact pads are patterned on top of the SOI substrates, which is then passivated by an overlayer of 500 nm PECVD oxide and followed by oxide CMP for global planarization. These Cu pads, with lateral dimensions on the order of 3-5 μm, are inconsequential in handle wafer bonding, but will eventually participate in device-device wafer bonding in Section 2.5.

Once passivated and planarized, the SOI substrate is ready for handle wafer attachment. On both the SOI substrate and the 100 nm LPCVD nitride handle wafer, 150 nm Zr and 300 nm Cu was deposited in sequence. With no need for wafer-wafer alignment, the SOI and the nitride handler were bonded at 400 ^{o}C in N_2 ambient with persistent contact pressure of 4000 mbar for 30 min. The pair underwent a further anneal at 400 ^{o}C in N_2, in which the Cu-Cu interface forms a strong bond that passes both the razor test [5,7] and subsequent mechanical substrate grinding.

2.2. Substrate Etchback and Backside Via Formation

With the handle wafer in place, the next task involves the complete removal of the SOI bulk Si using a combination of mechanical grindback and aqueous chemical etching, which will selectively stop on the 400 nm buried oxide (BOX) layer.

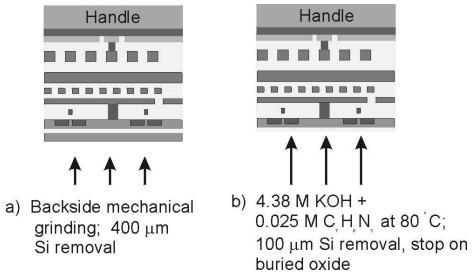

Figure 4. SOI etchback

To start, 400-420 μm of the SOI bulk was removed using grinding, while the remaining 80 to 100 μm of Si was etched in a solution containing 4.38 M (20% wt) KOH at 80 ^{o}C for approximately 2 hrs, which has a Si-to-oxide selectivity of about 300 : 1. In addition, at the same KOH concentration, Zr is virtually impervious to hydroxide attack until the solution temperature reaches beyond 120 ^{o}C. Last, but not least, the 100 nm LPCVD nitride layer provides a near-perfect protection of the handle wafer against KOH attack.

Although Cu has excellent corrosion resistant to alkaline (except for ammonia and other Cu chelates) solutions of all concentrations at room temperature, the metal will undergo some oxidation at environments above 50-60 ^{o}C. With our 4.38 M KOH solution at 80 ^{o}C, we have observed spurious spots of Cu-Cu interface delamination at the wafer edges. This delamination situation seems to be ubiquitous - it also occurs in TMAH (tetramethylammonium hydroxide) or EDP (ethylenediamine with 1,2-benzenediol and water) etches of similar concentration and temperature [8,9]

There are two ways to prevent such Cu corrosion: One can either reduce the exposure time to hydroxide attack, or one can add a Cu corrosion inhibitor to the etch solution. Currently, we can completely suppress Cu-Cu interface corrosion by adding 0.025 M tolyltriazole ($C_7H_6N_3$, monopotassium salt) without sacrificing the Si-to-oxide selectivity, but at the expense of a 10 μm/hr decrease in the Si etch rate.

From Figure 5, upon completion of SOI substrate removal, inter-layer vias are created by etching through the BOX, SOI, and ILD 1, finally stopping on metal layer M1. This is followed by PECVD oxide sidewall passivation and via filling using a damascene process. As shown in Figure 1, a typical via aspect ratio is around 2:1, with a via width about 0.5 μm.

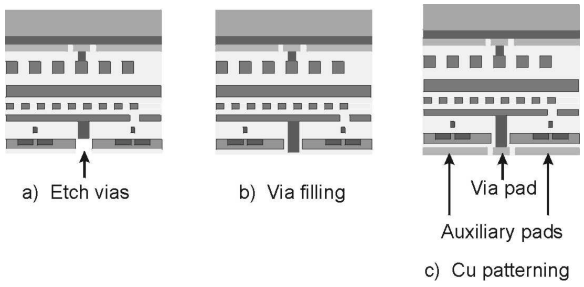

Figure 5. Backside via and Cu/Ta pad formation

Finally, (300 / 50 nm) thick Cu/Ta pads, with lateral dimensions on the order of 3 to 5 μm, are patterned right on top of the inter-layer vias. Auxiliary Cu pads, which has no role in inter-wafer communication, can also be patterned to increase the total surface area for subsequent Cu-Cu wafer bonding.

2.3. Wafer-Wafer Alignment and Bonding

The thinned SOI substrate in Figure 5, complete with backside inter-layer vias and Cu bond pads, is now ready to be bonded to another CMOS device wafer, presumably

also with its own set of multilevel interconnects and Cu/Ta bond pads that mirror those of the thinned SOI.

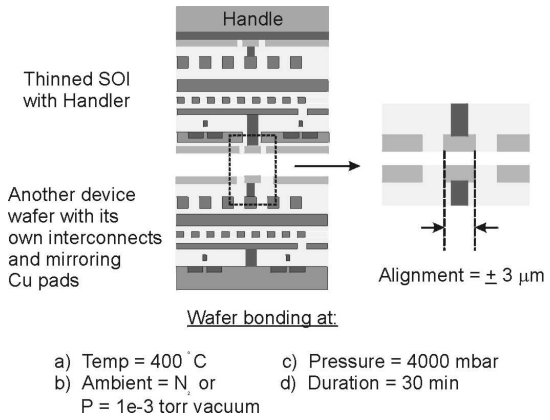

Figure 6. Creation of a 3-D stack

Both wafer-to-wafer alignment and bonding were performed in the Electronic Vision EV 450 Aligner and AB1-PV Bonder [5,7]. Since the system has an inherent ± 3 μm mis-alignment, any Cu/Ta bond pads less than or equal to 3 μm are unacceptable. Thus, wafer-to-wafer alignment is the ultimate factor in determining the inter-layer via density. With better optical alignment systems, it is possible to decrease the Cu/Ta pad sizes down to around 0.5 to 1 μm, which corresponds to a substantial increase in via density.

When the wafers were properly aligned, the pair was clamped and transferred to the bonding chamber, where both substrates were heated to 400 ^{o}C in N_2 ambient and hot-pressed for 30 min under 4000 mbar of pressure. Further anneal at 400 ^{o}C for 30 min in N_2 completes the Cu-Cu bond.

2.4. Handle Wafer Release

The final step of our 3-D integration scheme is releasing the handle wafer from the top SOI layer.

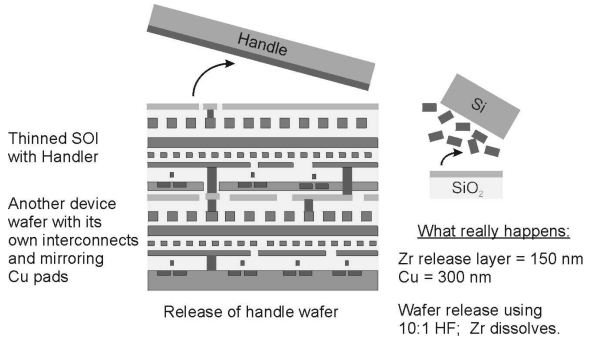

Figure 7. Handle wafer release with dilute HF

Recalling from Section 2.1, the nitride handle wafer was attached to the SOI substrate with a Zr/Cu - Cu/Zr bond. To destroy this metal bond, one can immerse the wafer stack in a dilute 10:1 water:HF solution. Zirconium, like Ti, succumbs to HF attack at an extremely high rate, much higher than the rate of SiO_2 degradation. With vigorous agitation, Zr undercutting across the whole wafer can occur in about 10 to 15min, thereby releasing the nitride handler from the finished 3-D stack. Further dipping of the 3-D stack in dilute HF will expose the Cu/Ta bond pads created earlier in Section 2.1. On a side-note, Ti was not used as the release layer because it is rigorously attacked by KOH around and above 80 ^{o}C.

Now, referring back to Figure 2, the finished 3-D stack, with the Cu/Ta pads exposed, can immediately be bonded to another thinned SOI substrate, just like in Figure 6, and thus exhibiting the parallelism, process repeatability and robustness of this 3-D integration scheme.

3. Characteristics of the Cu-Cu Bond

In the MIT 3-D scheme, the Cu-Cu bonding interface serves both as a "glue" layer and electrical contact points between different device planes. Therefore, reliability of the Cu-Cu bond, in terms of both its mechanical and electrical properties, is of most importance. Initial results on determining the Cu-Cu interface specific contact resistance has shown great promises, but more work needs to be done to fully characterize the electrical properties of the bond. This is because electrical data for contact resistance is skewed when the Cu-Cu bond is physically homogeneous, in which the Cu-Cu bonding interface is absent (i.e. this constitutes a perfect bond, and IR drops across a non-existent interface is difficult to extract and differentiate from "bulk" Cu backgrounds).

On the other hand, there are several articles in the literature that have investigated both the mechanical properties and possible bonding mechanisms of the Cu-Cu interface [7]. Our current work has produced a mechanically reliable Cu-Cu bond at 400 ^{o}C, with minimal metal oxidation at the interface - sometimes no oxidation at all (oxygen content lower than 3 wt % in EDS analysis). Upon further elucidation of the bonding mechanism in the future, one could better optimize the bonding process in order to meet various fabrication criteria for a given 3-D circuit, such as lower bonding temperature, etc.

4. Circuit-Design Tools for 3-D Integration

No circuit fabrication technology is commercially viable without tools that allow designers to develop circuits using the technology. A number of tools have been developed or are in progress that can be used, for example, to generate masks, or to take a higher-level schematic and target it for fabrication in 3-D. As this technology matures, the on-going work in this area will ensure that circuit designers are capable of utilizing the advantages 3-D has to offer.

5. Summary

This paper summarized the MIT 3-D integration process flow, and presented a brief discussion on the most important reliability issues.

6. Acknowledgements

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7. References

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