Errata

(Last Updated December, 2006)

- p.6, line 5: “difficulty” => “difficult”
- p.8, 2nd paragraph under Summary: “mutual exclusive” => “mutually exclusive”
- p.16, last line: “EAD” => “EDA”
- p.31, VHDL code line 24: i1=>sig1, i2=>a(2)
- p.53, 4th line: “VHDL is a known” => “VHDL is known”
- p.54, Table 3.1: “srl” => “sra” (shift-right arithmetic)
- p. 56, section 3.5.2, 1st paragraph: “Theses data ...” => “These data …”
- p.62, last paragraph, 3rd sentence: "to_intger" => "to_integer"
- p.65, 2nd line: delete “them”
- p.69, section 4.1: “term” = > “terms”
- p.72, 3rd line from bottom: “show” => “shown”
- p.73, 2nd paragraph , 3rd sentence: “std_logic data type” => “the std_logic data type”
- p.74, 2nd paragraph, 1st sentence: “highest” => “the highest”
- p.75, 1st line in “Simple ALU” subsection: “scr0” => “src0”
- p.109, bottom 14th line : “sig_b <= value_expr_b_1” => “sig_b <= value_expr_b_1;”
- p.110, pseudo code: “signal_a” => “sig” to match notation in Figure 5.5
- p.125, 2nd line from bottom: “The” => “ This”
- p.137, 1st paragraph: “back-plan” => “back-plane”
- p.144, aoi cell: “the area is 11” => “the area is 10”
- p.153, 1st line: “in realty” => “in reality”
- p.154, Figure 6.18: label “area” and “delay” for x and y axis
- p. 155, last paragraph, 2nd sentence: “… in at the RT level” =>: “… at the RT level”

- p. 163, 2nd paragraph, last sentence: “architectural”=> “architecture”
- p. 218, section 8.2.2, "Timing analysis" subsection, 2nd sentence: “combination” => “combinational”.
- P. 219, section 8.2.3, “Regular sequential circuit” subsection, last sentence: “and shifter” => “and a shifter”.
- P.240, section 8.6.1, last paragraph: “issue is be discussed” => “issue is discussed”
- p. 243, section 8.6.4, 6th sentence: “output”=> “outputs”.
- p. 246, 1st sentence: “The interpretation the code” => “The interpretation of the code”
- p. 258, Figure 9.1: “r_req” => “r_reg”
- p. 260, Figure 9.2: “r_req” => “r_reg”
- p. 315, 2nd paragraph: “condition” => “conditional”
- p. 330, Figure10.14: “resset” => “reset”
- p. 333, Figure10.15: “resset” => “reset”
- p. 337, Figure10.17: “resset” => “reset”
- p.353, section 10.8.2, 2nd paragraph, line 5: “resources” => “resource”
- p. 377, 3rd paragraph, 1st line: “las” => “as”
- p. 377, last paragraph, 4th line: “timing diagrams is” => “timing diagram is”
- p.387, Figure 11.8: “a_req, n_req, r_rq” => “a_reg, n_reg, r_reg”
- p.398, Figure 11.11: “a_req, n_req, r_rq” => “a_reg, n_reg, r_reg”
- p. 404, 3rd paragraph, 3rd line : “FSDM” => “FSMD”
- p. 412, Listing 11.7, line 62: “a_next(0)” => “b_next(0)
- p. 415, Figure 11.19, add_shift state: “n←next” => “n←n_next”
- p. 424, line 2: “consider a mod-5 counter” => “consider as a mod-5 counter”
- p. 430, section 12.3.1, 6th line: “cs” => “ce”
- p. 430, section 12.3.1, 2nd paragraph, 4th line: “cs” => “ce”

- p. 430, section 12.3.1, 2nd paragraph, 7th line: “cs” => “ce”
- p. 432, Figure 12.5: “cs” => “ce”
- p. 432, Figure 12.6: “cs” => “ce”
- p. 456, Figure 12.22(b), state s1: “r3 ← abs(r1)” => “r1←abs(r1)”
- p 626, Figure 16.12: “strectcher”=> “stretcher”
- p. 637, 7th line: “the the” => “the”
- p. 639, 2nd line: “The revised the talker …” => “The revised talker …”