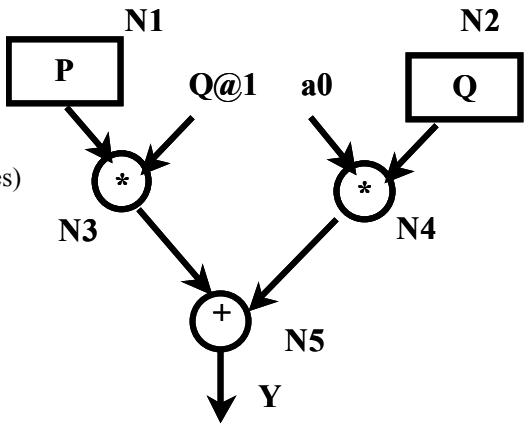
EE 4743 Test #2 Solutions – Fall 2002

For any partial credit, you must show your work.

1. (25 pts) The flowgraph below implements the equation:
Y = Q@1 * P + a0 * Q. Assume that a0 is already preloaded into a register. For the flowgraph below,

a. Show a schedule that will use one multiplier, one adder, and only one input bus for inputting the Q, P values. Use as few clock cycles as possible, and you cannot chain operations. Do not use any overlapped computations (i.e, a computation must be finished before you can input new P, Q values). Multiplication and adders units do not have pipeline stages. You may not need all the clock cycles shown in the table.

You must show register allocation!! You cannot use more than three registers (R1, R2) in addition to the register needed for a0.



b. Give the required resources (# of adders, # of multipliers, # of input busses) required in order to produce a schedule that produces the Y value with the lowest possible latency as seen from the flowgraph.

Minimum latency from flowgraph is 3 clocks.
2 input busses, 2 multipliers, 1 adder.

	Multiplier	**Adder**	**Register transfer ops**
Clk 1			R1 ← P
Clk 2	N3 (Q@1=R2 * P=R1)		R2 ← Q (overwrite old Q@1) R1 ← N3 (overwrite P)
Clk 3	N4 (a0* Q=R2)		R3 ← N4
Clk 4		N5 (N3=R1 + N4=R3)	
Clk 5			
Clk 6			

2. (20 pts) For the flowgraph in problem 1, used overlapped computations to achieve an initiation rate faster than what can be achieved without overlapped computations. You can use as many multipliers, adders as you wish, but you can still only use one input bus for the P, Q values. Execution units do not have pipeline stages.

   a. What is the latency of your schedule? 4

   b. What is initiation rate? 2

   c. How many multipliers are needed? 1

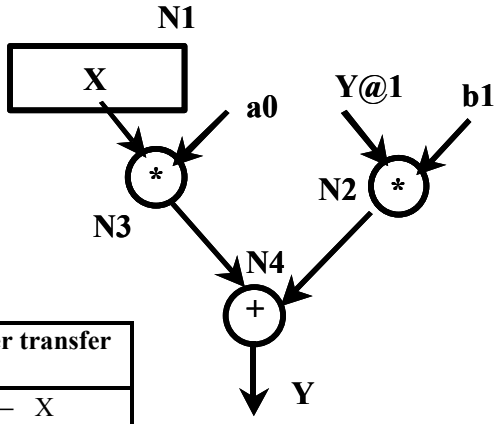
   d. How many adders are needed? 1

Cannot start overlap in Clk2 because only one input bus!!!!

	Sample J	Sample J+1	Sample J+2	Sample J+3	Sample J+4
Clk 1	N1				
Clk 2	N3, N2				
Clk 3	N4	N1			
Clk 4	N5	N3,N2			
Clk 5		N4	N1		
Clk 6		N5	N3,N2		
Clk 7			N4		
Clk 8			N5		
Clk 9					
Clk 10					
Clk 11					
Clk 12					
Clk 13					
Clk 14					

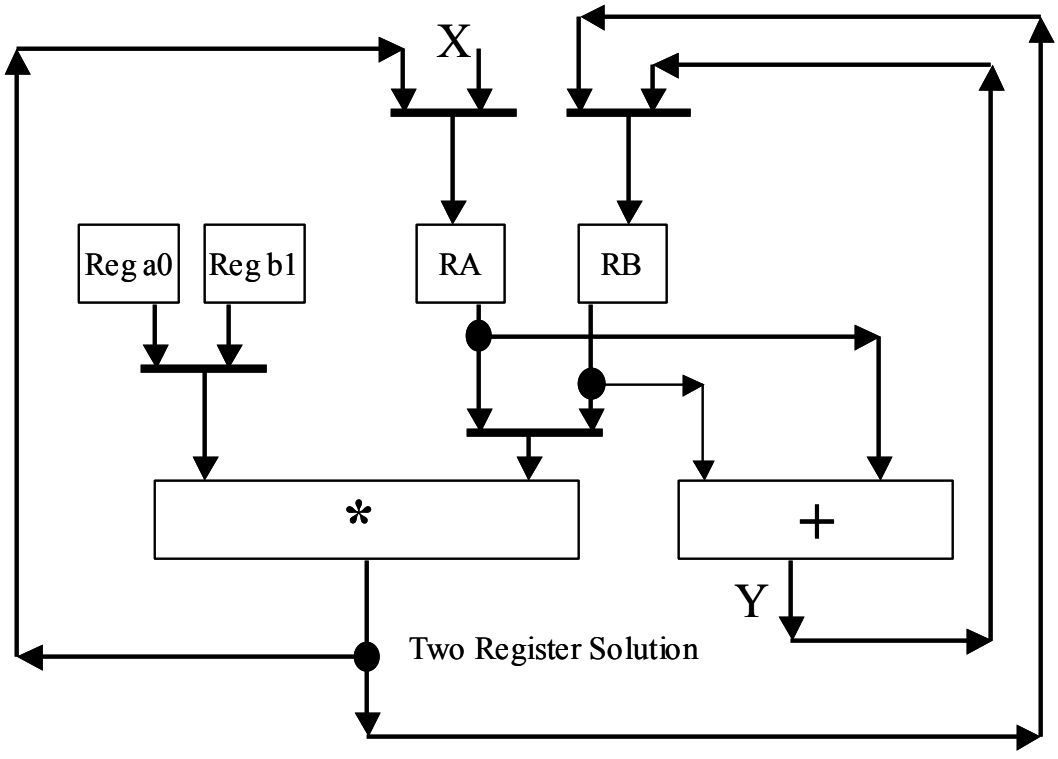
3. (20 pts) A schedule and datapath is shown for the flow graph below. Draw an ASM chart that implements the control for this datapath. Assume that the control waits for a START input to be asserted before beginning computations, and that new X values are available when your control needs them (you do not need handshaking for inputting new X values). When the START input is negated, finish the last computation and return to the first state where the controller waits for assertion of START.

Figure 1

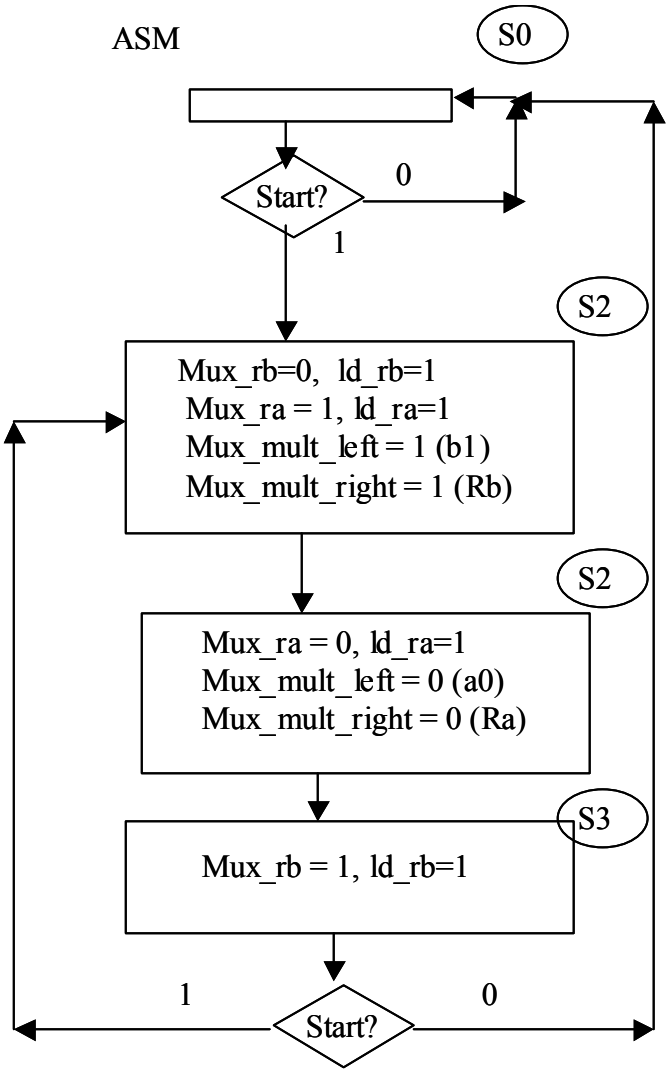


Your ASM chart MUST clearly show all control lines required in the data path below. Draw your ASM chart on the next page.

	Multiplier	**Adder**	**Register transfer ops**
Clk 1	N2 (RB=Y@1 * b1)		RA ← X RB ← N2
Clk 2	N3 (RA=X * a0)		RA ← N3
Clk 3		N4 (RB=N2 + RA=N3)	RB ← N4



ASM Chart required for Problem #3:



Mux names:

Mux_ra, Mux_rb

mux_mult_left, mux_mult_right

All mux inputs: Left = 0, Right = 1

4. (10 pts). For the datapath given in problem #3, delays are as follows:

TCQ of register: 3 ns
Tsu of register: 2 ns
Thd of register: 1 ns
Tpd of Mux: 6 ns
Tpd of adder: 11 ns
Tpd of multiplier: 16 ns

a. What is the minimum clock period time for this datapath?

TCQ + Tmux + Tmult + Tmux + Tsu = 3 + 6 + 16 + 6 + 2 = 33 ns

b. What could you do to this datapath to reduce the clock period time. Be specific!!

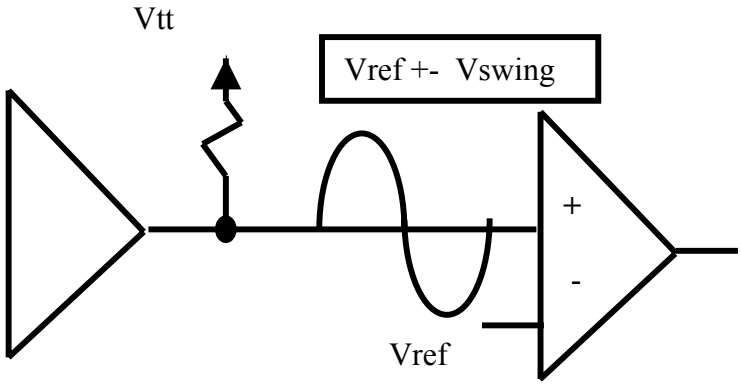
Pipeline the execution units (multiplier, adder).

Answer 6 of the next 9 problems: (24 pts) CROSS OUT THE PROBLEMS THAT YOU DO NOT WANT GRADED!

5. How does an open-drain output work?

   Can pull low or high impedance.

6. Draw the basic scheme for a Voltage-referenced IO.



7. What is the noise advantage of a differential voltage IO over a Voltage-referenced IO.

   Rejects common mode noise.

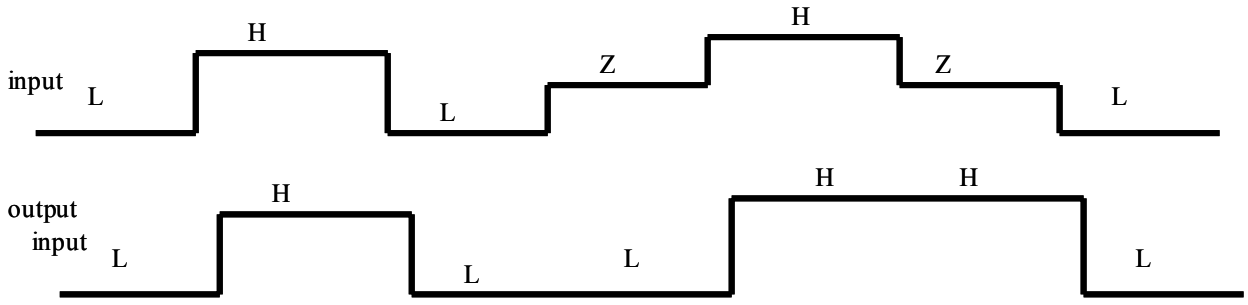
8. What does a source-synchronous protocol mean? Why is it useful?

   Transmits clock with data so that wire delays do not affect timing.

9. What new architectural feature for speeding up addition did the Altera Stratix FPGA offer over the Altera FLEX FPGA?

   Carry Select Adder scheme

10. If the *bus-keeper* circuit is used on an output of an Altera IO circuit, fill in the timing diagram below for the *output* given the input value to the bus keeper circuit (H=high, L=low, Z= high impedance, draw a short propagation delay for changes in the output value).



output

When Z input, keeps last driven value.

11. IO elements in FPGAs have a method for controlling output slew. Give two reasons why is it important to control output slew rate.

    Reduce inrush current which reduces noise; reduce signal corruption from reflections

12. Assume FSM A wants to transfer data to FSM B via a common SRAM memory. What is the minimum number of clocks required to transfer 20 words if a single ported SRAM is used? What is the minimum number of clocks required to transfer 20 words if a true dual-ported SRAM is used?

    The true dual ported RAM will allow the transfer in about half the time (40 clocks versus 20 clocks) since we can both read and write in the same clock cycle.

13. Two new features were implemented on the Altera Stratix FPGA that makes it attractive for DSP applications. What were they?

    Here are three:
    - *Monolithic Multipliers*
    - *A monolithic accumulator*
    - *true dual port RAMs*