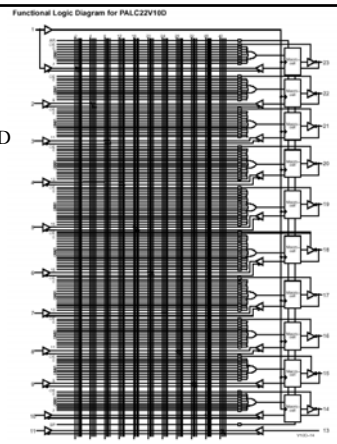
Programmable Logic

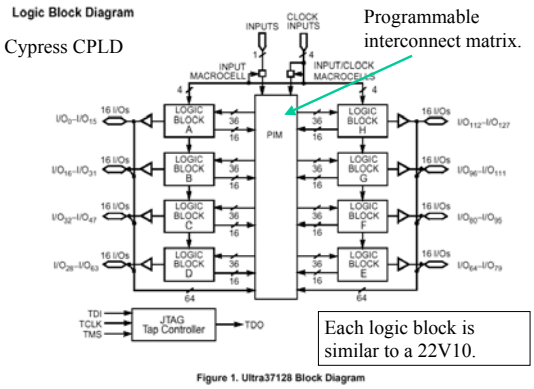
- So far, have only talked about PALs (see 22V10 figure next page).
- What is the next step in the evolution of PLDs?
  - More gates!
- How do we get more gates? We could put several PALs on one chip and put an interconnection matrix between them!!
  - This is called a Complex PLD (CPLD).

22V10 PLD



Cypress CPLD

Programmable interconnect matrix.

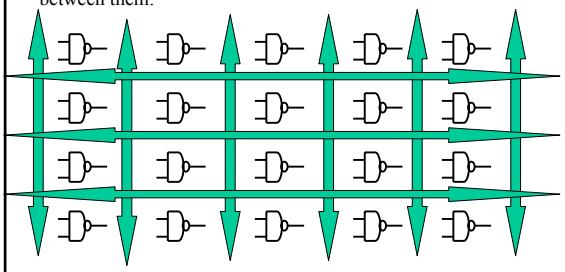


Each logic block is similar to a 22V10.

Figure 1. Ultra37128 Block Diagram

Any other approaches?

Another approach to building a "better" PLD is place a lot of primitive gates on a die, and then place programmable interconnect between them:



Field Programmable Gate Arrays

The FPGA approach to arrange primitive logic elements (logic cells) arrange in rows/columns with programmable routing between them.

What constitutes a primitive logic element? Lots of different choices can be made! Primitive element must be classified as a "complete logic family".

- A primitive gate like a NAND gate
- A 2/1 mux (this happens to be a complete logic family)
- A Lookup table (I.e, 16x1 lookup table can implement any 4 input logic function).

Often combine one of the above with a DFF to form the primitive logic element.

Other FPGA features

- Besides primitive logic elements and programmable routing, some FPGA families add other features
- Embedded memory
  - Many hardware applications need memory for data storage. Many FPGAs include blocks of RAM for this purpose
- Dedicated logic for carry generation, or other arithmetic functions
- Phase locked loops for clock synchronization, division, multiplication.

Altera Flex 10K FPGA Family

Table 1. FLEX 10K Device Features

Feature	EPF10K10 EPF10K10A	EPF10K20	EPF10K30 EPF10K30A	EPF10K40	EPF10K50 EPF10K50V
Typical gates (logic and RAM), *Note (1)*	10,000	20,000	30,000	40,000	50,000
Usable gates	7,000 to 31,000	15,000 to 63,000	22,000 to 69,000	29,000 to 93,000	36,000 to 116,000
Logic elements (LEs)	576	1,152	1,728	2,304	2,880
Logic array blocks (LABs)	72	144	216	288	360
Embedded array blocks (EABs)	3	6	6	8	10
Total RAM bits	6,144	12,288	12,288	16,384	20,480
Maximum user I/O pins	134	189	246	189	310

Altera Flex 10K FPGA Family (cont)

Table 2. FLEX 10K Device Features

Feature	EPF10K70	EPF10K100 EPF10K100A	EPF10K130V	EPF10K250A
Typical gates (logic and RAM), *Note (1)*	70,000	100,000	130,000	250,000
Usable gates	46,000 to 118,000	62,000 to 158,000	82,000 to 211,000	149,000 to 310,000
LEs	3,744	4,992	6,656	12,160
LABs	468	624	832	1,520
EABs	9	12	16	20
Total RAM bits	18,432	24,576	32,768	40,960
Maximum user I/O pins	358	406	470	470

Note to tables:

(1) For designs that require JTAG boundary-scan testing, the built-in JTAG circuitry contributes up to 31,250 additional

Figure 1. FLEX 10K Device Block Diagram

Dedicated memory

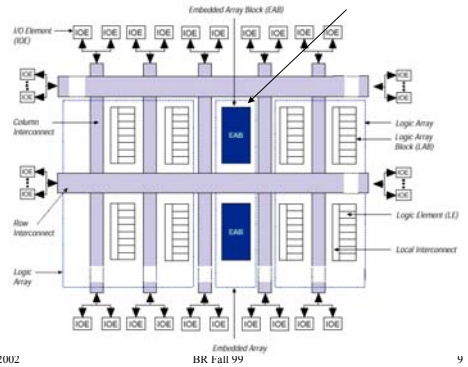
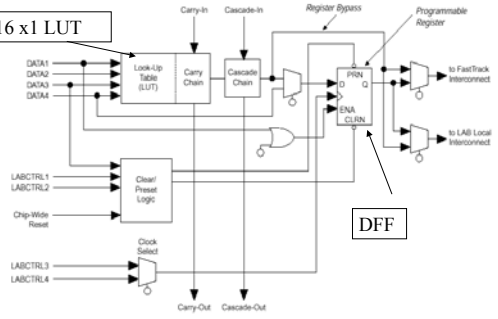


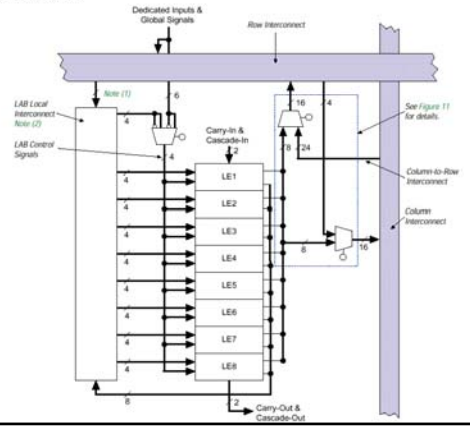
Figure 6. FLEX 10K Logic Element

16 x1 LUT



DFF

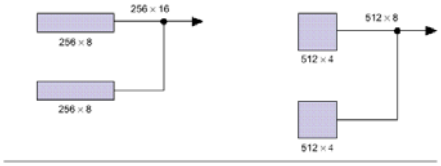
Figure 5. FLEX 10K LAB



Emedded Array Block

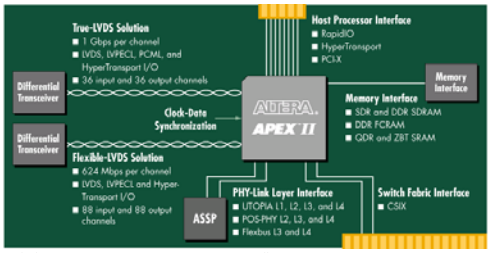
- Memory block, Can be configured:
  - 256 x 8, 512 x 4, 1024 x 2, 2048 x 1

Figure 3. Examples of Combining EABs

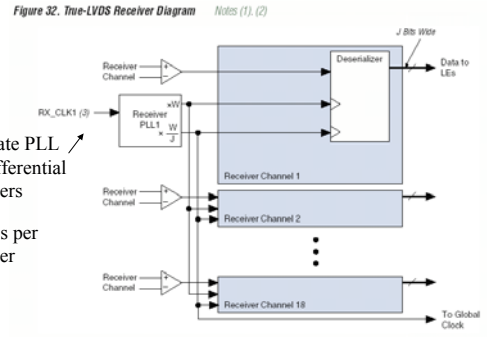


Altera APEX II

- Altera's latest FPGA family is the APEX II
- Latest addition is support for high speed serial transfer protocols, embedded processor cores



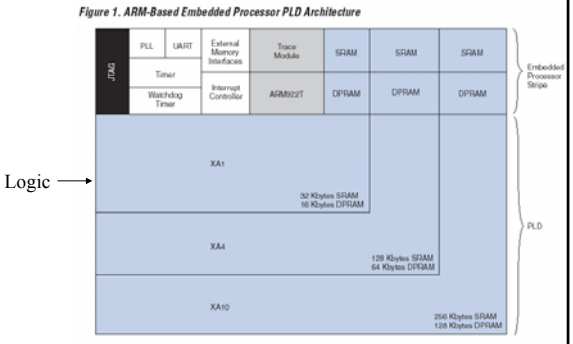
Differential Serial IO support in APEX II



Separate PLL for differential receivers

1 Gbps per receiver

Altera Excalibur device has embedded processor + programmable logic.



Altera NIOS processor IP block

- An IP (Intellectual Property) block is some functional block such as a PCI bus interface, processor, etc specified in an RTL and mapped to an FPGA implementation
  - Altera licenses IP based on their FPGAs so companies do not have to re-invent the wheel
- NIOS softcore processor specs:
  - Load/store RISC architecture
  - Datapath size of 16 or 32 bits
  - 16 bit instruction set
  - 5 stage pipeline
  - Up to 512 registers (windowed, 32 visible)
  - 13% of Apex 20K200 device (16 bit datapath), 20% in 32-bit datapath configuration
  - User can add custom instructions

Issues in FPGA Technologies

- Complexity of Logic Element
  - How many inputs/outputs for the logic element?
  - Does the basic logic element contain a FF? What type?
- Interconnect
  - How fast is it? Does it offer 'high speed' paths that cross the chip? How many of these?
  - Can I have on-chip tri-state busses?
  - How routable is the design? If 95% of the logic elements are used, can I route the design?
    - More routing means more routability, but less room for logic elements

Issues in FPGA Technologies (cont)

- Macro elements
  - Are there SRAM blocks? Is the SRAM dual ported?
  - Is there fast adder support (i.e. fast carry chains?)
  - Is there fast logic support (i.e. cascade chains)
  - What other types of macro blocks are available (fast decoders? register files?)
- Clock support
  - How many global clocks can I have?
  - Are there any on-chip Phase Logic Loops (PLLs) or Delay Locked Loops (DLLs) for clock synchronization, clock multiplication?

Issues in FPGA Technologies (cont)

- What type of IO support do I have?
  - TTL, CMOS are a given
  - Support for mixed 5V, 3.3v IOs?
    - 3.3 v internal, but 5V tolerant inputs?
  - Support for new low voltage signaling standards?
    - GTL+, GTL (Gunning Tranceiver Logic) - used on Pentium II
    - HSTL - High Speed Transceiver Logic
    - SSTL - Stub Series-Terminate Logic
    - USB - IO used for Universal Serial Bus (differential signaling)
    - AGP - IO used for Advanced Graphics Port
  - Maximum number of IO? Package types?
    - Ball Grid Array (BGA) for high density IO

Altera FPGA Family Summaries

- Altera Flex10K/10KE
  - LEs (Logic elements) have 4-input LUTS (look-up tables) +1 FF
  - Fast Carry Chain between LE's, Cascade chain for logic operations
  - Large blocks of SRAM available as well
- Altera Max7000/Max7000A
  - EEPROM based, very fast (Tpd = 7.5 ns)
  - Basically a PLD architecture with programmable interconnect.
  - Max 7000A family is 3.3 v

Xilinx FPGA Family Summaries

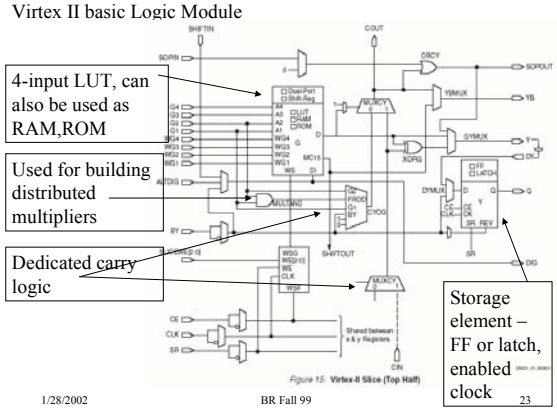
- Virtex Family
  - SRAM Based
  - Largest device has 1M gates
  - Configurable Logic Blocks (CLBs) have two 4-input LUTS, 2 DFFs
  - Four onboard Delay Locked Loops (DLLs) for clock synchronization
  - Dedicated RAM blocks (LUTs can also function as RAM).
  - Fast Carry Logic
- XC4000 Family
  - Previous version of Virtex
  - No DLLs, No dedicated RAM blocks

Xilinx Virtex II Family

- Virtex II is Xilinx's latest & greatest
- New technology:
  - embedded multipliers 18x18=36 bit, 2's complement (signed multiplier)
  - Differential serial IO
- Multiplier inputs are linked to embedded SRAM outputs for speed.
  - Intended to be used for digital filter applications where sample cofficient values are stored in the SRAM
- A FIR filter (finite impulse response) equation has the form $y = x * a0 + x[1]*a1 + x[2]*a2 + \ldots X[N-1]* aN-1$

The 'x' values are previous sample values (x[1] is one sample back), the 'a' values are coefficient.

Virtex II basic Logic Module



Actel FPGA Family Summaries

- MXDS Family
  - Fine grain Logic Elements that contain Mux logic + DFF
  - Embedded Dual Port SRAM
  - One Time Programmable (OTP) - means that no configuration loading on powerup, no external serial ROM
  - AntiFuse technology for programming (AntiFuse means that you program the fuse to make the connection).
  - Fast (Tpd = 7.5 ns)
  - Low density compared to Altera, Xilinx - maximum number of gates is 36,000

Actel ProAsic basic logic module

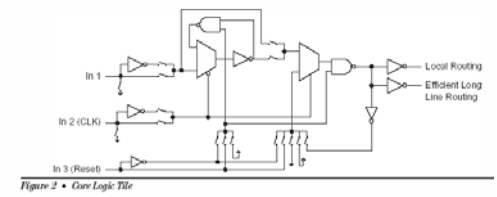


Figure 2 • Core Logic Tile

Extremely primitive logic module (fine-grain architecture). Mux is basic building block – two muxes shown can implement a DFF via a master/slave latch arrangement.

Cypress CPLDs

- Ultra37000 Family
  - 32 to 512 Macrocells
  - Fast (Tpd 5 to 10ns depending on number of macrocells)
  - Very good routing resources for a CPLD