EE 3714 Test #1 Solutions- Spring 2000 – Reese

1. (5 pts) What is the minum number of bits that I need if I want to encode 33 distinct items?
   ***6** bits ($2^6 = 64$)*
2. (5 pts) What range of signed integers can I represent using 4 bits and 2's complement representation?
   -8 to 7
3. (5 pts) The following 8-bit hex number $E7 represents a signed integer in 2's complement format. What is its decimal value? *$E7 is a negative number, complement & Add one, get $19. Convert to decimal, get **25**.*

4. (5 pts) The following 8-bit hex number $3A represents a signed integer in signed magnitude format. What is its decimal value? *This is a positive number, convert to decimal: **58**.*

5. (5 pts) Convert the following number decimal -21 (negative twenty-one) to an 8-bit representation using one's complement format. *Convert magnitude to hex: $15. Complement, get: **$EA**.*

6. (5 pts) How do you detect overflow when adding 2's complement number?
   Add two negative numbers, get positive. Add two positive numbers, get negative.

7. (5 pts) How do you detect overflow when adding unsigned numbers?
   Carry out of most significant bit position.

8. (5 pts) Convert the following expression to a POS form:
   AC+D(B+E) = (AC +D)(AC+B+E) = (A+C)(A+D)(A+B+E)(C+B+E)

9. (5 pts) Write the truth table for the following function: F (A,B,C) = (AB)' + C

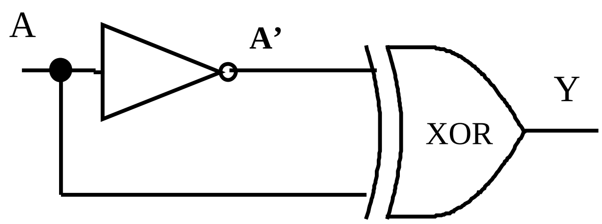
A B C	(AB)'	(AB)' + C
0 0 0	1	1
0 0 1	1	1
0 1 0	1	1
0 1 1	1	1
1 0 0	1	1
1 0 1	1	1
1 1 0	0	0
1 1 1	0	1

10. (5 pts) Simplify the following equation to as few terms as possible
    AB' + AB'CD + ABC'D'

Hint: the relation X + X'Y = X + Y is useful. Also final answer has two product terms, one term with 2 variables, the other term with 3 variables.

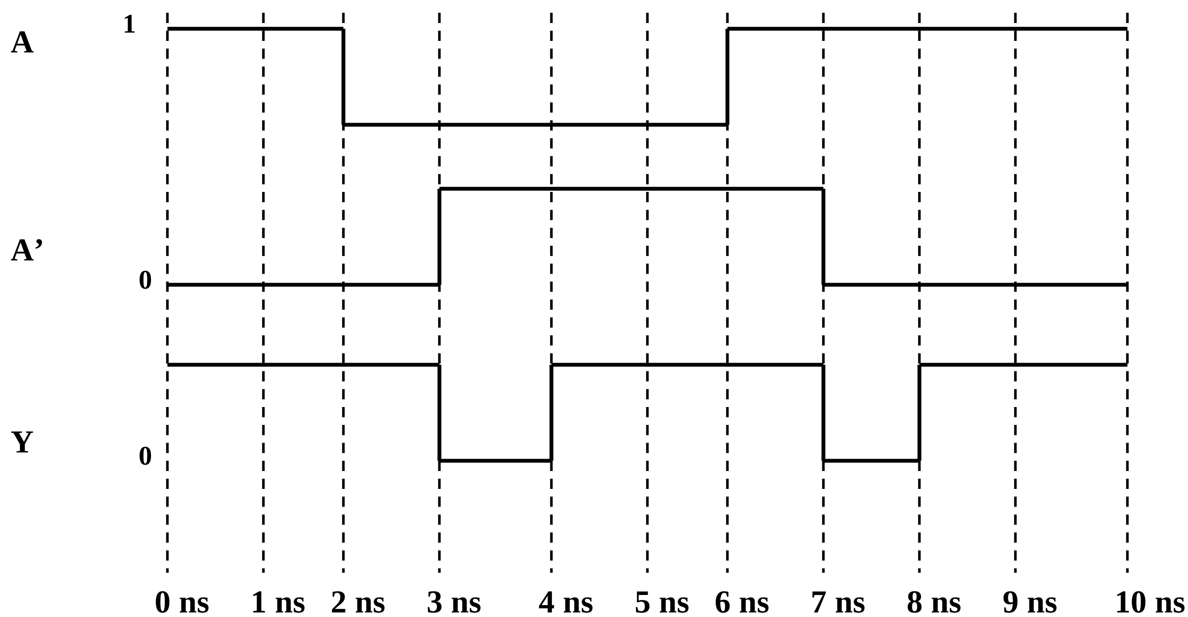
AB' (1 + CD) + ABC'D'
AB' + ABC'D'
A(B' + BC'D')
A(B' + C'D')
AB' + AC'D'

11. (10 pts) Complete the timing diagram for the A', Y signals. Each gate has a delay of 1 ns. Complete the diagram out to 10 ns.



XOR

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0



12. (5 pts) Draw the CMOS transistor diagram for a 2 input NOR gate. *SEE NOTES.*

13. (5 pts) Used DeMorgan's Law on the following equation until the NOT operator is only applied to single variables:

$$(X'Y + A'(B+C))' = (X'Y)'(A'(B+C))'$$
$$= (X+Y')((A')' + (B+C)')$$
$$= (X+Y')(A + B'C')$$

14. (5 pts) In the circuit shown below, what is the MAXIMUM path delay if the propagation delay of the inverters is 1 ns, the AND gate propagation delay is 2 ns, and the OR gate propagation delay is 5 ns?

19 ns, SEE FIGURE 2.14(b) pg 38 in textbook.

15. (5 pts) Which two level gate forms are used to directly implement boolean equations in POS equations? (hint: You need to list '2' two level gates forms*)* *OR-AND, NOR-NOR*

16. (5 pts) Which two level gate forms are used to directly implement boolean equations in SOP equations? (hint: You need to list '2' two level gates forms) *AND-OR, NAND-NAND*

17. (5 pts) Explain the terms 'wafer' and 'die' in terms of integrated circuit manufacturing.
Wafer is a thin, round (6-8") piece of silicon that is processed thru the fabrication line. Each Wafer is divided into rectangular areas called 'die' -each die contains the same integrated circuit.

18. (5 pts) Explain the terms 'fanout' and 'fanin'.
Fanin - number of gate inputs, Fanout - number of inputs that a particular output is connected to.

19. (5 pts) Convert the following expression to a SOP form that has only two product terms.

$$(A + BCD')(A' + D)$$
$$AA' + AD + A'BCD' + BCDD'$$
$$0 + AD + A'BCD' + 0$$
$$AD + A'BCD'$$