EE 3714 Test #1 SOLUTIONS - Fall 2001 – Reese

Student ID: _____ (no names please)

Work all problems.   Closed book, closed notes; No calculators.You may use the supplied reference
material.

1. (9 pts) Convert the decimal value below to its 8-bit representation in each of the following encoding
    schemes.   Write your answers in either HEX (base 16) or binary.

|	Signed Magnitude	1's Complement	2's Complement
-29 *hex magnitude = 1D* *(16 + 13)*	*9D = 10011101*	*E2 = 11100010*	*E3=11100011*

2. (5 pts) Repetitively apply De'Morgan's theorem to the equation until only single variables are
    complemented (the not operator is applied only to single variables).

$$((A' + B'C) D)' = (A' + B'C)' + D'$$
$$= A (B'C)' + D'$$
$$= A(B+C') + D'$$
$$= AB + AC' + D'$$

3. (5 pts)   Simplify the following equation to a minimal expression:

$$AB + ABC + B$$
$$B (A + AC + 1)$$
$$B$$

4. (5 pts) Use one or more gates below such that Y is a LOW voltage when either button A or button B
    is pressed. Be sure to give gate numbers such as 7400, 7432, 7402, 7408, 7404 etc.
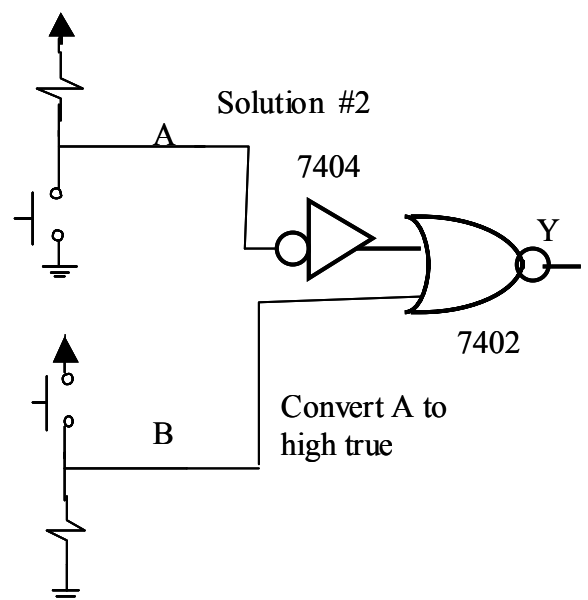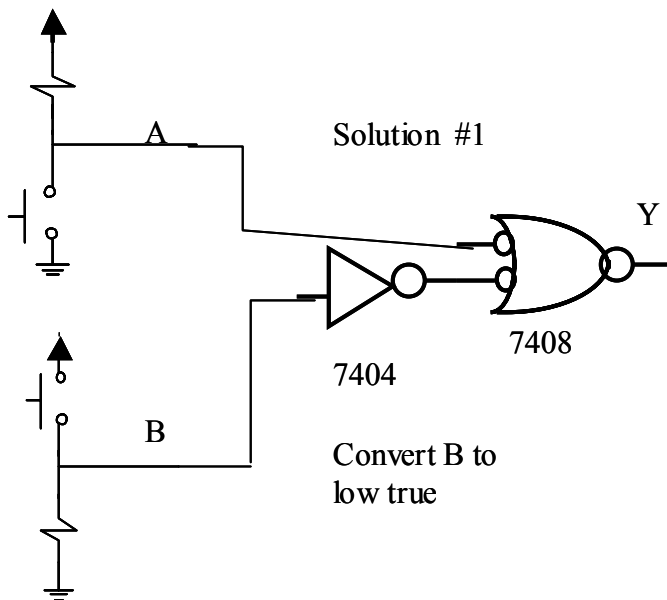
5. (5 pts) Complete the timing diagram below for A' and Y assuming that all gate delays = 1 ns.

A

A'

Y
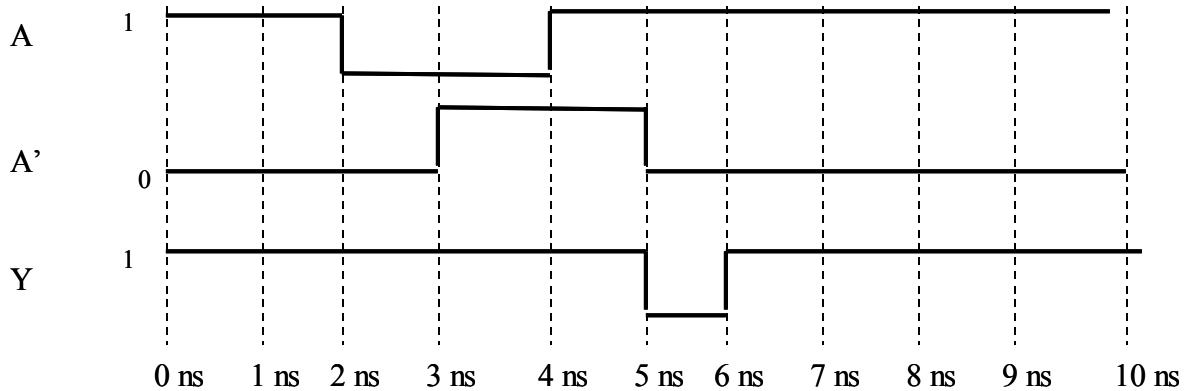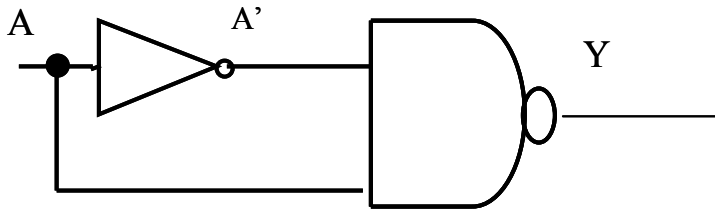
6.   (5 pts) Write the following function in SOP form using the minterms indicated. Do NOT minimize.

$F(A,B,C) = \Sigma$ m(1, 4, 6)   = A'B'C + AB'C' + ABC'

7.   (5 pts) Write the following function in POS form using the maxterms indicated. Do NOT minimize.

$F(A,B,C) = \Pi$ M(1, 4, 6) = (A+B+C')(A'+B+C)(A'+B'+C)

8. (5 pts) Write the MAXTERM POS form that represents the following truth table for F(A,B,C)

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Π M(0, 4, 6)
(A+B+C)(A'+B+C)(A'+B'+C)

9. (5 pts) What is the voltage value (L or H) of output Y when   A = L, B = H, C =H.   To get credit for this problem, you MUST show which transistors are open or closed and the path from Y to either Vdd or Gnd.

B=H

A=L

Vdd

C= H

Vdd

Y = L

B=H

A=L

C=H
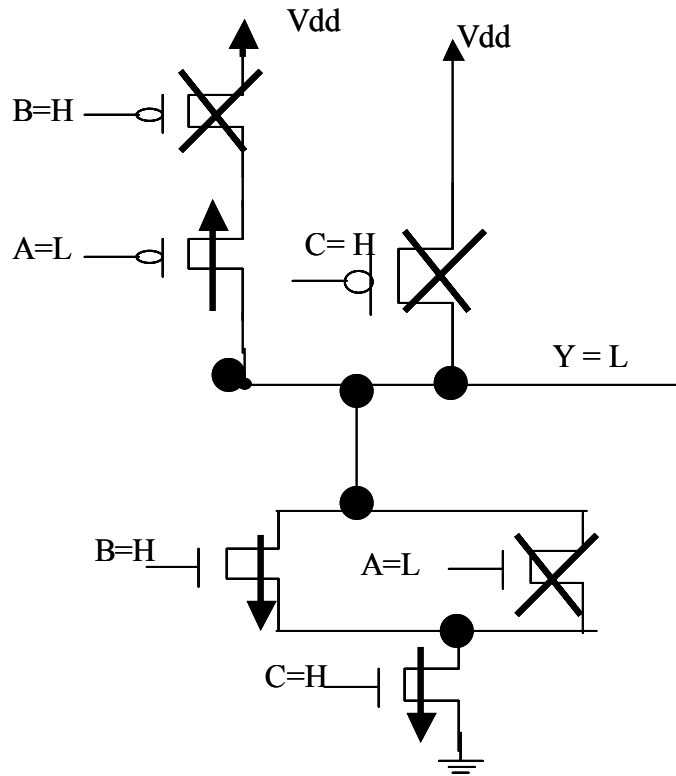
10. (5 pts) Fill in the truth table for the following function: F (A,B,C) = (A+B)' C

$$F = (A+B)'C = A'B'C$$

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

11. (6 pts) Using the following gates: 7432, 7400, 7408, 7402, 7404   give three combinations that are 'complete' logic families.   Your three combinations of complete families cannot overlap.

   Family #1: _____7400 (NAND gates are complete)_____

   Family #2: _____7402 (NOR gates are complete)_____

   Family #3: _____7408,7404   OR   7432, 7404_____

12. (8 pts) PROVE or DISPROVE the following Boolean theorem. You can either use truth tables or algebraic manipulation. You MUST show your work.

$$(A \text{ xor } B) \, C \;=\; (AC) \text{ xor } (BC)$$

$$(AB' + A'B) \, C \;=\; (AC)(BC)' + (AC)'(BC)$$

$$AB'C + A'BC \;=\; AC(B'+C') + (A'+C')BC$$
$$= AB'C + ACC' + A'BC + BCC'$$
$$= AB'C + 0 + A'BC + 0$$
$$= AB'C + A'BC$$

   PROVED .

A	B	C	(A xor B) C	(AC) xor (BC)
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	1
1	0	0	0	0
1	0	1	1	1
1	1	0	0	0
1	1	1	0	0

13. (12 pts) Use one of the following terms to fill in the blanks below (you can also use numbers such as '1', '2', '3', etc).

CMOS   DIE   WAFER   PMOS   NMOS   TTL TPHL   TPLH
        POWER   FREQENCY   ASCII   XOR   NAND   NOR   PACKAGES
HIGH   LOW   ASCII

a.   ___CMOS_____ gates consist of PMOS and NMOS transistors.

b. The ___TPLH_____ delay is the time delay between a low to high voltage change on the output and a change on an input.

c. A CMOS 2-input NAND gate has _____4_____ transistors.

d. A ____WAFER_____ is cut up into small squares call 'die', and each die is placed in a package - the package is normally what people refer to as a 'chip'.

e. It would take _____5_____ binary digits to encode 17 distinct items.

f. The _____ASCII_____ code is a common method for encoding alphanumeric data.

14. (5 pts) Fill in the blanks in the following binary sequence if the sequence represents a GREY code (each code in the sequence is Boolean adjacent)

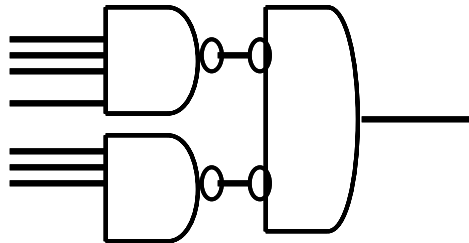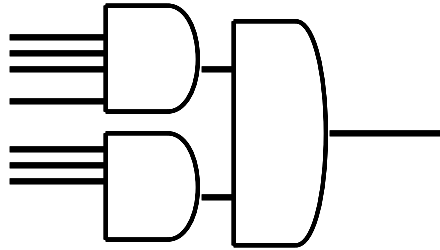000, 001, ___011____, 010, __110_____, 111, 101, ___100_____

15. (5pts) What is the sum of the following 8-bit Hex numbers?

$$\$ \ 7E \ + \ \$ \ 42 \ = \ \_\_\_\_\_\$ \ C0_____$$

16. (10 pts) I would like to implement an 8-input AND gate (F = A B C D E F G H) but I only have gates with 4 or fewer inputs. The gate types you have available are NAND, NOR, AND, OR, NOT.

Draw TWO different gate networks that implement this function. The gate types used in the two networks MUST BE DIFFERENT (i.e. if you use both NANDs and NORs in one network, they cannot be used in the other network).

And gates

NAND gates + NOR gate