# 6 *Simplification of Boolean Functions*

This experiment demonstrates the relationship between a Boolean function and the corresponding logic diagram. The Boolean functions and their **complements** are simplified by using **Karnaugh Maps**. The logic is implemented using only NAND gates.

NOTE: The PRELAB for this lab has Altera MAXPLUS simulation requirements. See the Prelab sheets for more information.

# I. Overview

The gate ICs to be used for the logic diagrams must be from the following list.

7400 2-input NAND.

7404 Inverter (1-input NAND).

7410 3-input NAND.

If an input to a NAND gate is not used, it should not be left open but instead should be connected to the logic supply through a resistor (1K). For example, if the circuit needs an inverter and there is an extra 2-input NAND gate available in a 7400 IC, then one input of the gate is connected as an inverter and the other is tied to a logic 1.

*NOTE: Also, both inputs could be tied together but this increases the load on the source. An additional option exists where an unused gate is available. The unused gate input(s) may be connected to ground and its output used to supply logic 1 to inputs of other gates.*

# II. Logic Diagram

A. This part of the experiment starts with a given logic diagram from which we proceed to apply simplification procedures to reduce the number of gates and possibly the number of ICs. The logic diagram shown in Fig. 1 requires two ICs, a 7400 and a 7410. Note that the inverters for inputs x, y, and z are obtained from the remaining three gates in the 7400 IC. If the inverters were taken from a 7404 IC, the circuit would have required three ICs. Assign pin numbers to all inputs and outputs of the gates and connect the circuit with the x, y, z inputs going to three switches and the output F to an indicator lamp. Test the circuit by obtaining its truth table.

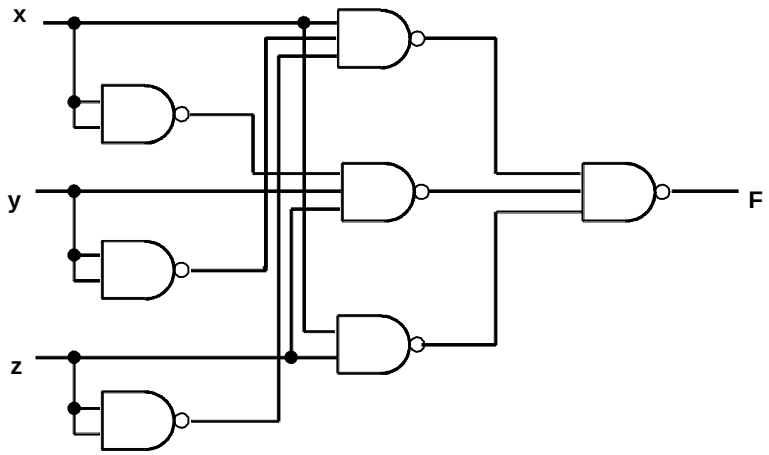


**Figure 1**

B. Obtain the Boolean function of the circuit and simplify it using the map method. Construct the simplified circuit without disconnecting the original circuit. Test both circuits by applying identical inputs to both and observing the separate outputs. Show that for each of the eight possible input combinations, the two circuits have identical outputs. This will prove that the simplified circuit behaves exactly as the original circuit.

# III. Boolean Functions

A. Given the two Boolean functions as sum of minterms:

$F_1 (A,B,C,D) = \Sigma\, m(0,1,4,5,8,9,10,12,13)$

$F_2 (A,B,C,D) = \Sigma\, m(3,5,7,8,10,11,13,15)$

Simplify the two functions by means of maps. Obtain a composite logic diagram with four inputs, A, B, C, D, and two outputs, $F_1$ and $F_2$. Implement the two functions together using a minimum number of NAND ICs. Do not duplicate the same gate if the corresponding term is needed for both functions. Use any extra gates in existing ICs for inverters when possible.

B. Connect the circuit and check its operation. The truth table for $F_1$ and $F_2$ obtained from the circuit should conform with the minterms listed above.

# IV. Complement

Plot the following Boolean function in a map:

F = A'D + BD + B'C + AB'D

Combine the 1's in the map to obtain the simplified function for F in sum of products. Then combine the 0's in the map to obtain the simplified function for F' also in sum of products. Implement both F and F' using NAND gates and connect the two circuits to the same input switches but to separate output indicator lamps. Obtain the truth table of each circuit in the laboratory and show that they are the complements of each other.

# V. Report

Include the following sections of this experiment in the laboratory report.

A. Section II. Include a discussion of a trouble shooting strategy for the circuit of Fig. 6.1. Also, show how the simplification of F (produced using a map) can be obtained by algebraic means as well.

B. Section III.

C. Section IV. Also, discuss the effects of propagation delay on the relationship between F and F' of your circuit. Specifically examine the time difference of changes at F and F' for a given input variable transition.

Be certain to show IC pin numbers on all logic diagrams.

**PRE-LAB DATA SHEET** **TA CHECKOFF SIGNATURE_____**

Truth Table for Figure 1

| x | y | z | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | | | | | | | |
| 0 | 0 | 1 | | | | | | | |
| 0 | 1 | 0 | | | | | | | |
| 0 | 1 | 1 | | | | | | | |
| 1 | 0 | 0 | | | | | | | |
| 1 | 0 | 1 | | | | | | | |
| 1 | 1 | 0 | | | | | | | |
| 1 | 1 | 1 | | | | | | | |

Output F =

K-map for Figure 6.1

| X \ YZ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | | | | |
| 1 | | | | |

Simplified F =

| x | y | z | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | | | | | | | |
| 0 | 0 | 1 | | | | | | | |
| 0 | 1 | 0 | | | | | | | |
| 0 | 1 | 1 | | | | | | | |
| 1 | 0 | 0 | | | | | | | |
| 1 | 0 | 1 | | | | | | | |
| 1 | 1 | 0 | | | | | | | |
| 1 | 1 | 1 | | | | | | | |

NAND equivalent of F (Schematic) =

ALTERA MAXPLUS REQUIREMENTS: The ZIP archive with this lab contains a schematic called 'p2_a.gdf' that is the original circuit in Part II, Figure 1. You should simulate this and use the simulation to verify your prelab is correct. You must COMPLETE the Altera Maxplus schematic called 'p2_b.gdf' that is your simplified F function. You must also simulate this circuit. You should have a screenshot of your schematic + simulation of your simplified design to show the TA or else demo the design for the TA using a portable PC.

ALTERA SIMULATION CHECKOFF Part II:_____

**(Pre Lab continued)**

Boolean Functions and Complement. (may not need all columns)

| A | B | C | D | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | | | | | | | | | | |
| 0 | 0 | 0 | 1 | | | | | | | | | | |
| 0 | 0 | 1 | 0 | | | | | | | | | | |
| 0 | 0 | 1 | 1 | | | | | | | | | | |
| 0 | 1 | 0 | 0 | | | | | | | | | | |
| 0 | 1 | 0 | 1 | | | | | | | | | | |
| 0 | 1 | 1 | 0 | | | | | | | | | | |
| 0 | 1 | 1 | 1 | | | | | | | | | | |
| 1 | 0 | 0 | 0 | | | | | | | | | | |
| 1 | 0 | 0 | 1 | | | | | | | | | | |
| 1 | 0 | 1 | 0 | | | | | | | | | | |
| 1 | 0 | 1 | 1 | | | | | | | | | | |
| 1 | 1 | 0 | 0 | | | | | | | | | | |
| 1 | 1 | 0 | 1 | | | | | | | | | | |
| 1 | 1 | 1 | 0 | | | | | | | | | | |
| 1 | 1 | 1 | 1 | | | | | | | | | | |

K-maps

| | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | | | | |
| 01 | | | | |
| 11 | | | | |
| 10 | | | | |

| | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | | | | |
| 01 | | | | |
| 11 | | | | |
| 10 | | | | |

| | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | | | | |
| 01 | | | | |
| 11 | | | | |
| 10 | | | | |

| | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | | | | |
| 01 | | | | |
| 11 | | | | |
| 10 | | | | |

Simplified $F_1$ =

Simplified $F_2$ =

**(Pre Lab continued)**
NAND equivalent $F_1$ (schematic)

NAND equivalent $F_2$ (Schematic)

Total # of NAND gates used for $F_1$ and $F_2$ =

**(Pre Lab continued)**

F = A'D + BD + B'C + AB'D
Simplified F = Simplified F' =
NAND equivalent of F(schematic)

NAND equivalent of F' (schematic)

Total # of NAND gates used for F and F'=

ALTERA MAXPLUS REQUIREMENTS: The ZIP archive with this lab contains a schematic called 'p4_org.gdf' that is the original Boolean equation in Part IV. You must COMPLETE the Altera Maxplus schematic called 'p4_f1.gdf' that will be your equivalent NAND F function. You must also simulate this circuit and verify it produces the same results as the 'p4_org.gdf' circuit. You must COMPLETE the Altera Maxplus schematic called 'p4_f0.gdf' that will be your equivalent NAND F' function. You must also simulate this circuit and verify it produces the complement results of the 'p4_org.gdf' circuit You should have a screenshot of your schematic + simulation of your NAND F and NAND F' designs or use demo the design for the TA using a portable PC at the beginning of the prelab.

ALTERA SIMULATION CHECKOFF Part IV:_____

**LAB DATA SHEET**

Demonstrate your working circuits to the TA and get a check off for each one.

II.B Figure 6.1 F: _____ (TA Checkoff signature)

Figure 6.1 F': _____ (TA Checkoff signature)

III.B F1: _____ (TA Checkoff signature)

F2:: _____ (TA Checkoff signature)

IV. F1: _____ (TA Checkoff signature)

F2: _____ (TA Checkoff signature)