

Sequential Systems

- A **combinational system** is a system whose **outputs** depends only upon its **current inputs**.
- A **sequential system** is a system whose **outputs** depends on the **current inputs** and the system's **current state**.
- All systems we have looked at to date have been **combinational** systems.

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Flip-Flops/ Latches

- Latches and Flip-Flops are devices that can have two internal states (0,1)
- The output of a latch or a Flip-Flop (FF) is dependent upon its **CURRENT STATE** and **CURRENT INPUTS**.
- Latches and FFs are the simplest examples of sequential systems.

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Set/ Reset Nor Latch (SR Nor Latch)

S	R	Ps	Ns
L	L	Q	Q
L	H	X	L
H	L	X	H
H	H	X	-

Present State

S	R	Ps	Ns
0	0	Q	Q
0	1	X	0
1	0	X	1
1	1	X	-

Next State

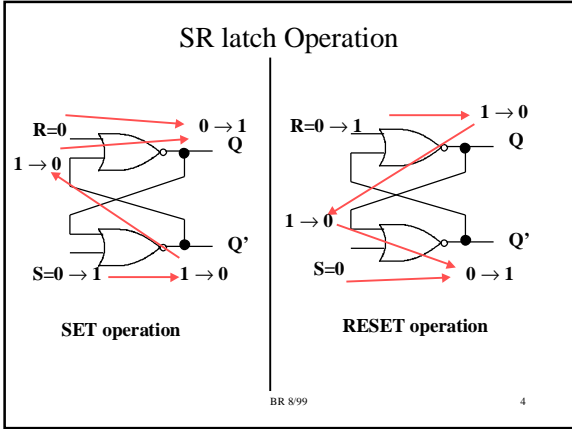
Implementation

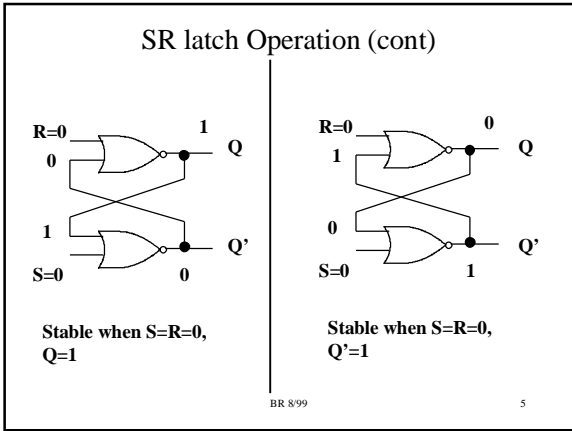
S	Q
R	Q'

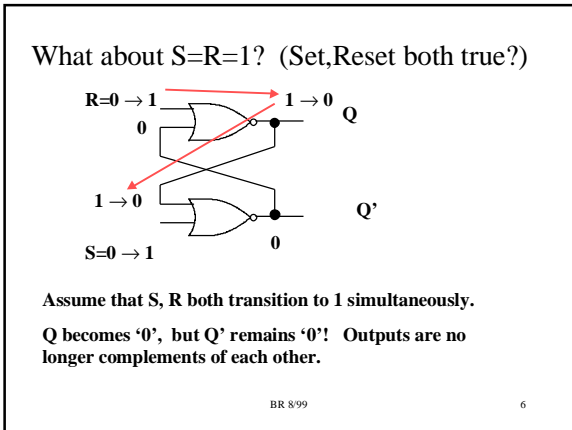
Symbol
inputs, outputs high true.

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What happens when S,R return to 0?

Oscillation occurs if S,R return to 0 simultaneously! At some point the system will settle into a stable condition. The bottom line is that S=R=1 is an illegal input condition (or design the SR latch such that one input is DOMINANT).

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SR Latch, R dominant

S	R	P _s	N _s
0	0	Q	Q
0	1	X	0
1	0	X	1
1	1	X	0

When S=R=1, then acts as a RESET (R is dominant)

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Set/ Reset Nand Latch (SR Nand Latch)

S	R	P _s	N _s
H	H	Q	Q
H	L	X	L
L	H	X	H
L	L	X	-

Present State

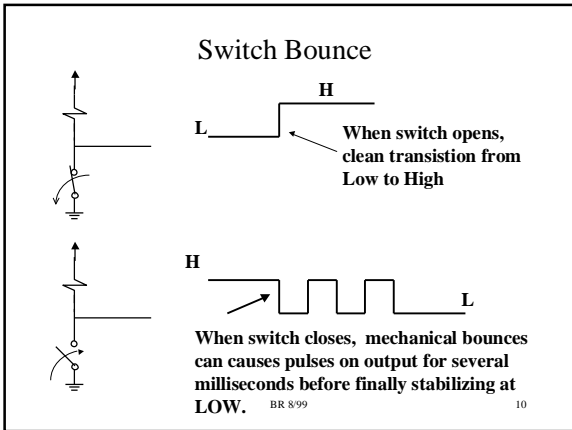
S	R	P _s	N _s
0	0	Q	Q
0	1	X	0
1	0	X	1
1	1	X	-

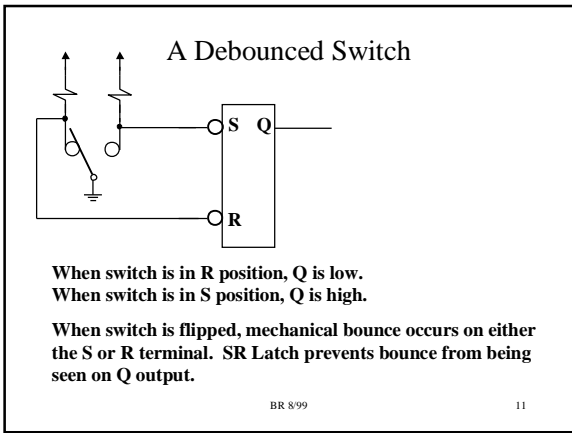
Next State

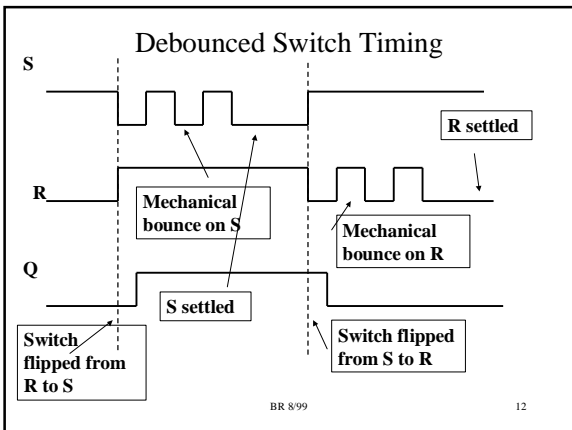
Implementation

Symbol inputs low true, outputs high true

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Terminology

- A *bistable memory device* is the generic term for the elements we are studying
- Can use the term **latch** or **flip-flop** to refer to these devices
 - latch: bistable memory device with level sensitive triggering (no clock)
 - flip-flop: bistable memory device with edge-triggering (with clock)
- **Warning:** Your author (Roth) uses the terminology **Flip-Flop** and **Clocked Flip-Flop** instead of latch and Flip-Flop
 - latch, flip-flop more standard

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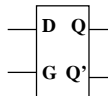
D-Latch (Data Latch)

G	D	Ps	Ns	Q
0	X	X	X	Q
1	0	X	X	0
1	1	X	X	1
1→0	D	1	X	D

When G=0, retain old value

When G=1, Q follows D (transparent mode)

When G=1→0 (falling edge), latch D value

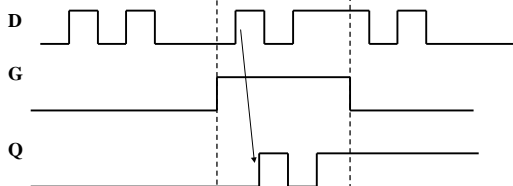


D is the Data input
G is the Gate input

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D-Latch Operation



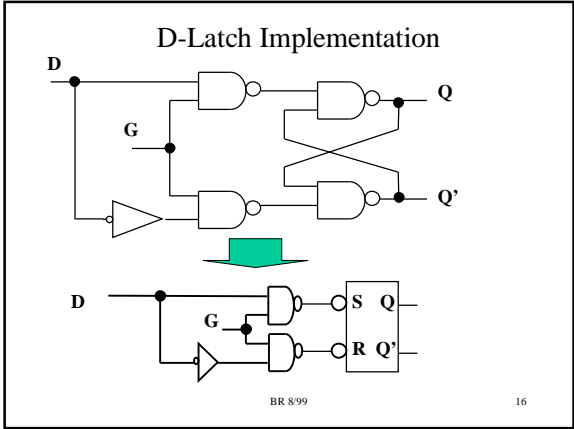
G is low, D has no effect on Q

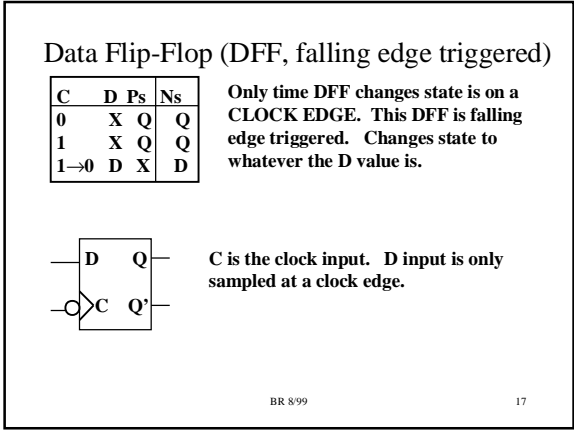
G is high, Q follows D (transparent mode)

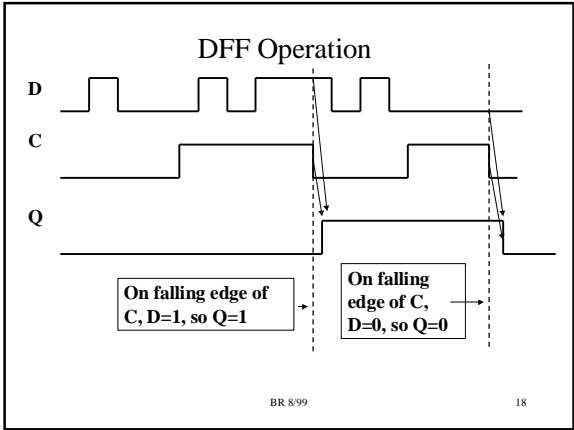
G is low, Q retains D value when G went 1→0

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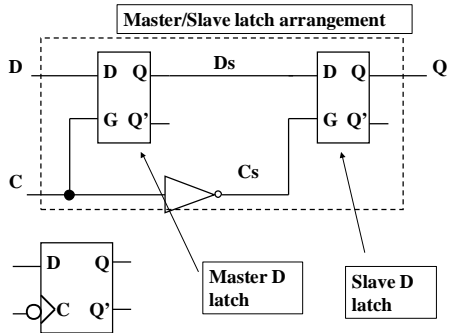
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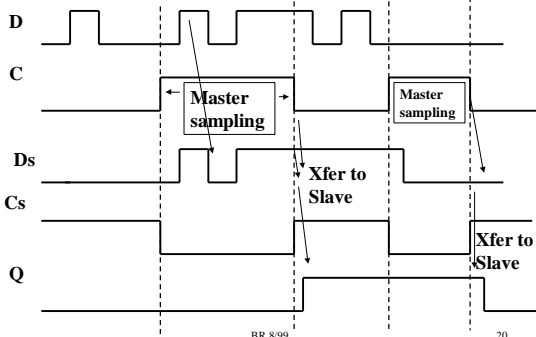
DFF Implementation (falling edge triggered)



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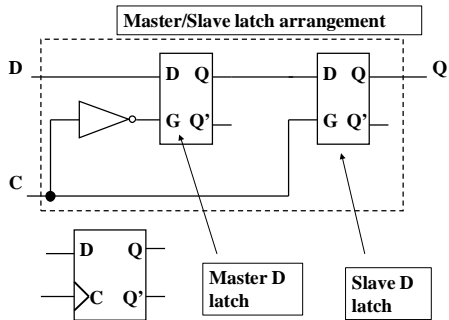
DFF Internal Operation



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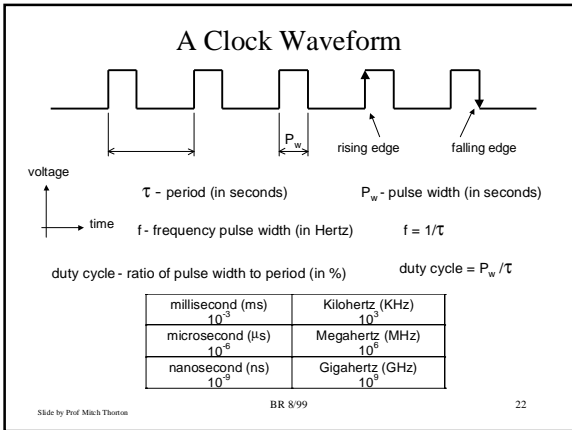
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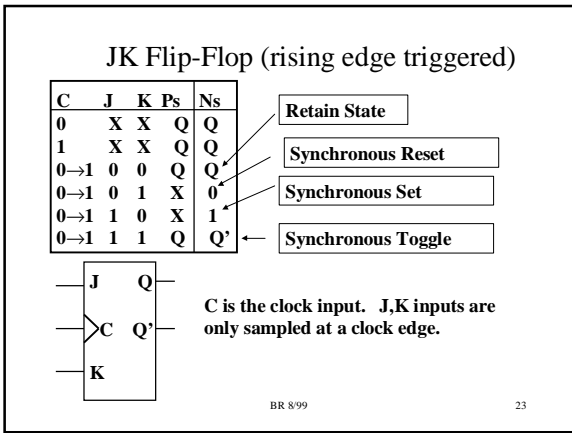
DFF Implementation (rising edge triggered)

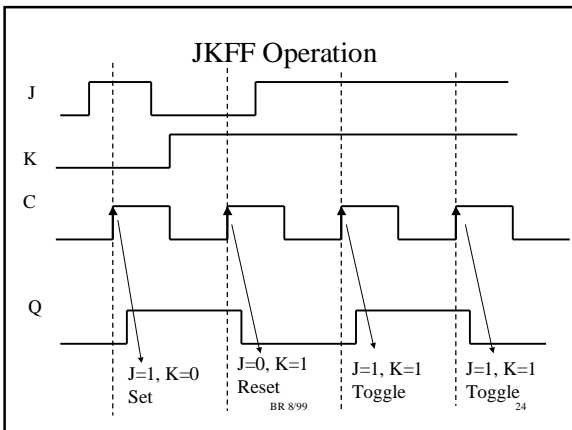


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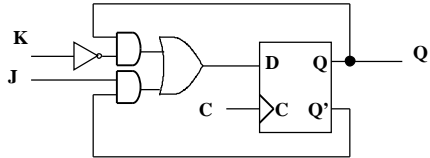
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JKFF Implementation



This is a rising edge triggered JK FF. Just substitute a falling edge triggered DFF to make a falling edge triggered JKFF.

We will derive this implementation at a later date.

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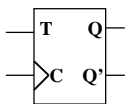
Toggle Flip-Flop (rising edge triggered)

C	T	Ps	Ns
0	X	Q	Q
1	X	Q	Q
0→1	0	Q	Q
0→1	1	Q	Q'

Retain State

Synchronous Toggle

TFF

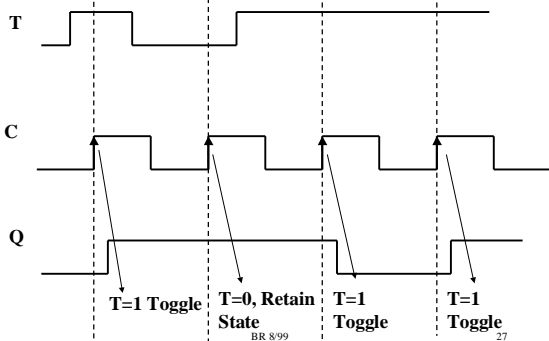


C is the clock input. T input only sampled at a clock edge.

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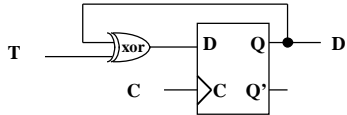
TFF Operation



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TFF Implementation



We will derive this implementation at a later date.

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What do you have to know?

- Definition of a sequential system
- SR Nand latch, SR Nor latch, D latch, DFF, JKFF, TFF
 - Operation all of the above
- Implementation of SR Nand, SR Nor, D latch, DFF
- Switch Debouncing
- Clock waveform characteristics

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