Lab 1 : Overview of the Xilinx Foundation Tools

Date: 9/14/04

Partner : Name of your lab partner

Prelab

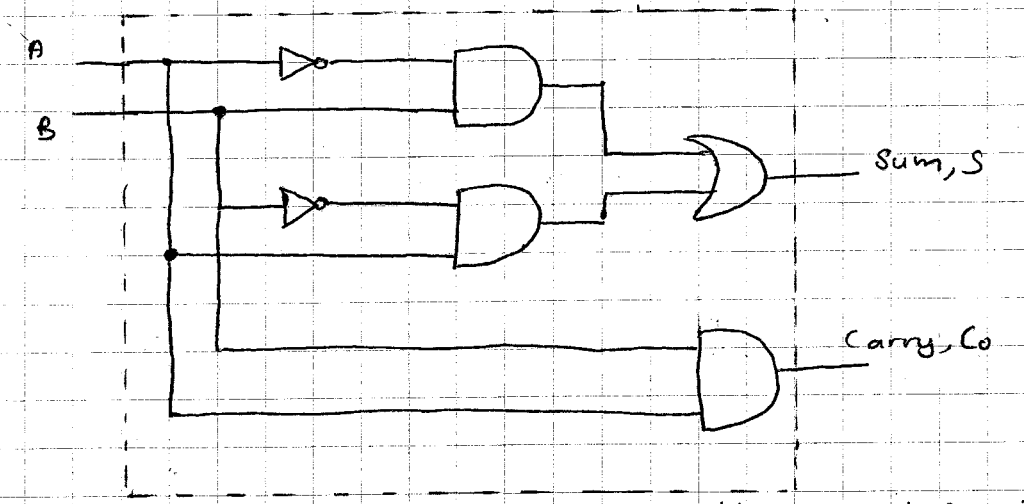

Figure 1: Schematic of a half adder circuit (HA)

Table for a half adder

Inputs			
A	B	Sum	Co
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

1. I read the section on Lab Safety
2. I read the section on "Design Flow Overview", "Devices" and "Project Manager
3. I read the section on "Entering a Schematic Design"
4. I read the section on "Functional ~~Sim~~ Simulation.

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In-Lab Experiment:

Objective: The goal of today's experiment is to build and simulate a half-adder circuit using the schematic Entry and functional simulator of Xilinx. This lab will help to understand the schematic entry tools and simulator interface of the Xilinx Foundation software.

Experimental Procedure

1. The schematic of the half adder circuit is entered using the Xilinx Foundation Tools. The logic gates are placed first and connected later. I/O pins for the two inputs A and B, and the outputs S and C_o, respectively are added. The schematic is saved.

Figure 1 below is a screenshot of the schematic of the half adder.

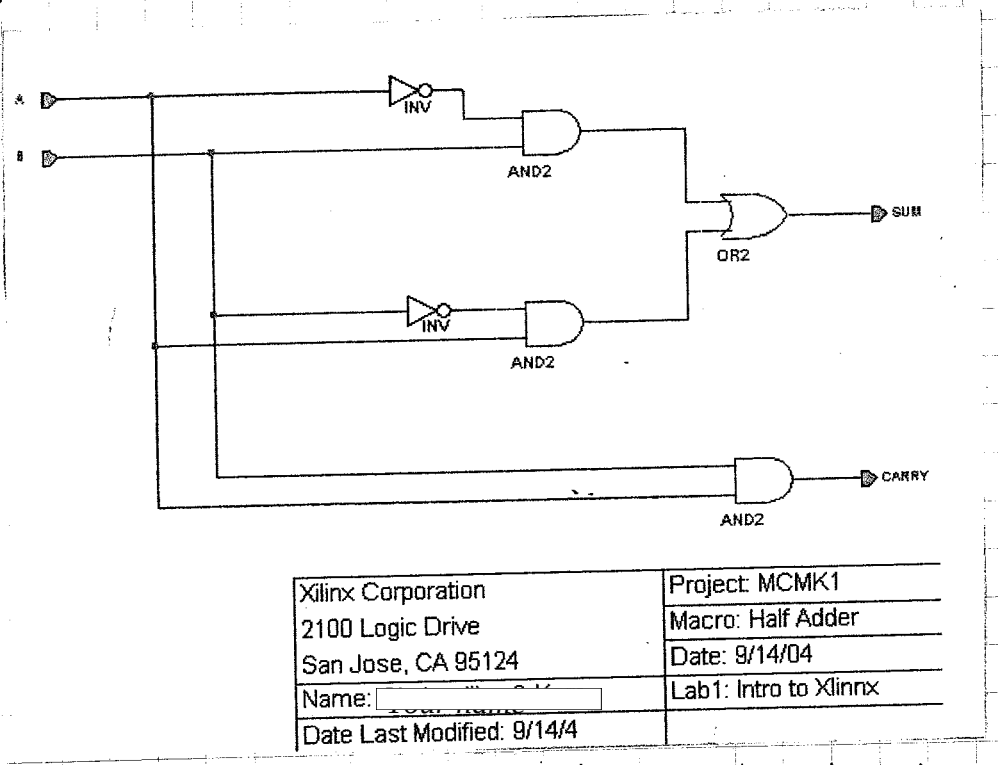
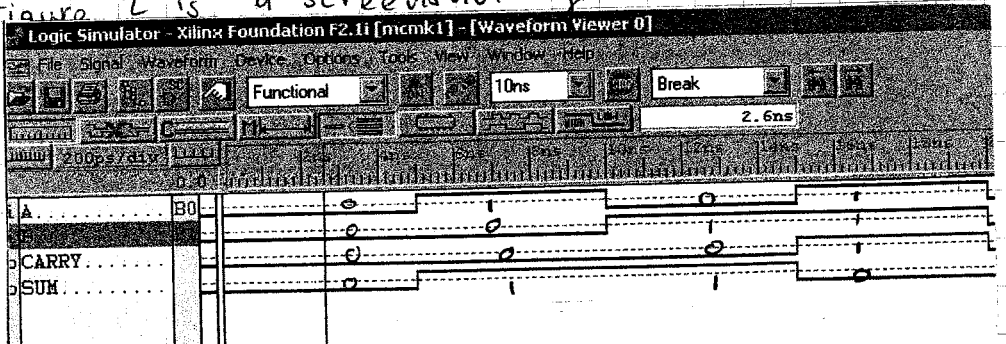


Fig 1: Schematic of half adder circuit entered using Xilinx Foundation Tools.

2. A functional simulation is done to check that the logic circuits give the required function.

Figure 2 is a screenshot of the simulation waveform.



According to the waveform in Fig 2, the truth table below is generated.

Time (ns)	Inputs		Outputs	
	A	B	Carry	Sum
0 – 5	0	0	0	0
5 – 10	1	0	0	1
10 – 15	0	1	0	1
15 – 20	1	1	1	0

Truth table according to Fig. 2

The inputs and their corresponding outputs are identical to the truth table in the prelab.
Thus, we get the right results for Sum and Carry and our circuit functions properly.

Discussion, conclusions:

1. We learned the operation of the half adder
2. We used Xilinx Schematic entry to implement the half adder circuit using logic gates
3. We verified the functional operation of the half adder using the logic simulator
4. The lab gave us an appreciation for the design and verification process in digital design.
5. We appreciated the fact that the Xilinx tools allowed us to design, test and debug the circuit.